HITACHI

SERVICE MANUAL

TK | No.9003E

DV-P305U
DV-P303U

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SPECIFICATIONS AND PARTS ARE SUBJECT TO CHANGE FOR IMPROVEMENT

DVD PLAYER

March 2000 Digital Media Products Division, Tokai

1. Precautions

1-1 Safety Precautions

1) Before returning an instrument to the customer, always make a safety check of the entire instrument, including, but not limited to, the following items:

(1) Be sure that no built-in protective devices are defective or have been defeated during servicing. (1)Protective shields are provided to protect both the technician and the customer. Correctly replace all missing protective shields, including any remove for servicing convenience.
(2)When reinstalling the chassis and/or other assembly in the cabinet, be sure to put back in place all protective devices, including, but not limited to, nonmetallic control knobs, insulating fish papers, adjustment and compartment covers/shields, and isolation resistor/capacitor networks. Do not operate this instrument or permit it to be operated without all protective devices correctly installed and functioning.

(2) Be sure that there are no cabinet openings through which adults or children might be able to insert their fingers and contact a hazardous voltage. Such openings include, but are not limited to, excessively wide cabinet ventilation slots, and an improperly fitted and/or incorrectly secured cabinet back cover.

(3) Leakage Current Hot Check-With the instrument completely reassembled, plug the AC line cord directly into a 120V AC outlet. (Do not use a isolation transformer during this test.) Use a leakage current tester or a metering system that complies with American National Standards institute (ANSI) C101.1 Leakage Current for Appliances and Underwriters Laboratories (UL) 1270 (40.7). With the instrument's AC switch first in the ON position and then in the OFF position, measure from a known earth ground (metal water pipe, conduit, etc.) to all exposed metal parts of the instrument (antennas, handle brackets, metal cabinets, screwheads, metallic overlays, control shafts, etc.), especially any exposed metal parts that offer an electrical return path to the chassis.
Any current measured must not exceed 0.5mA. Reverse the instrument power cord plug in the outlet and repeat the test. See Fig. 1-1.
Any measurements not within the limits specified herein indicate a potential shock hazard that must be eliminated before returning the instrument to the customer.

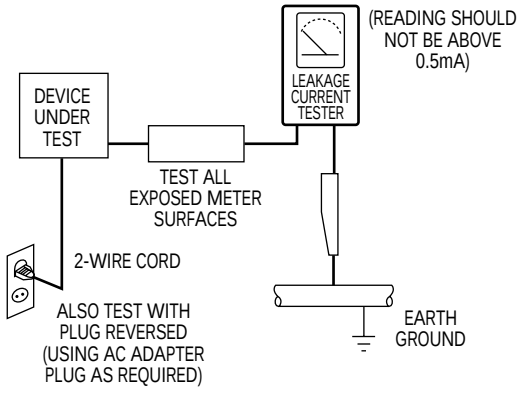


Fig. 1-1 AC Leakage Test

(4) Insulation Resistance Test Cold Check-(1) Unplug the power supply cord and connect a jumper wire between the two prongs of the plug. (2) Turn on the power switch of the instrument. (3) Measure the resistance with an ohmmeter between the jumpered AC plug and all exposed metallic cabinet parts on the instrument, such as screwheads, antenna, control shafts, handle brackets, etc. When an exposed metallic part has a return path to the chassis, the reading should be between 1 and 5.2 megohm. When there is no return path to the chassis, the reading must be infinite. If the reading is not within the limits specified, there is the possibility of a shock hazard, and the instrument must be re-pared and rechecked before it is returned to the customer. See Fig. 1-2.

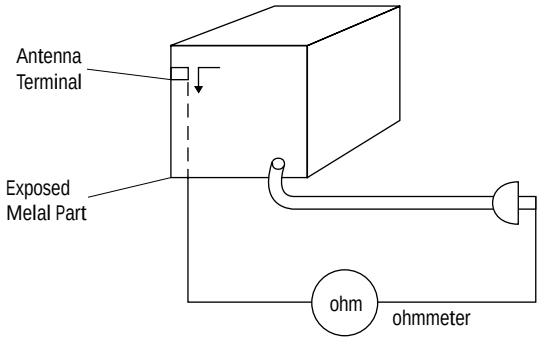


Fig. 1-2 Insulation Resistance Test

2) Read and comply with all caution and safety related notes non or inside the cabinet, or on the chassis.

3) Design Alteration Warning-Do not alter of add to the mechanical or electrical design of this instrument. Design alterations and additions, including but not limited to, circuit modifications and the addition of items such as auxiliary audio output connections, might alter the safety characteristics of this instrument and create a hazard to the user. Any design alterations or additions will make you, the service, responsible for personal injury or property damage resulting therefrom.

4) Observe original lead dress. Take extra care to assure correct lead dress in the following areas:
(1) near sharp edges, (2) near thermally hot parts (be sure that leads and components do not touch thermally hot parts), (3) the AC supply, (4) high voltage, and (5) antenna wiring. Always inspect in all areas for pinched, out-of-place, or frayed wiring, Do not change spacing between a component and the printed-circuit board. Check the AC power cord for damage.

5) Components, parts, and/or wiring that appear to have overheated or that are otherwise damaged should be replaced with components, parts and/ or wiring that meet original specifications.
Additionally, determine the cause of overheating and/or damage and, if necessary, take corrective action to remove any potential safety hazard.

6) Product Safety Notice-Some electrical and mechanical parts have special safety-related characteristics which are often not evident from visual inspection, nor can the protection they give necessarily be obtained by replacing them with components rated for higher voltage, wattage, etc. Parts that have special safety characteristics are identified by shading, an (⚠)or a (⚠)on schematics and parts lists. Use of a substitute replacement that does not have the same safety characteristics as the recommended replacement part might created shock, fire and/or other hazards. Product safety is under review continuously and new instructions are issued whenever appropriate.

1-2 Servicing Precautions

CAUTION : Before servicing Instruments covered by this service manual and its supplements, read and follow the Safety Precautions section of this manual.

Note : If unforseen circument create conflict between the following servicing precautions and any of the safety precautions, always follow the safety precautions. Remember: Safety First.

1-2-1 General Servicing Precautions

(1) a. Always unplug the instrument's AC power cord from the AC power source before (1) re-moving or reinstalling any component, circuit board, module or any other instrument assembly, (2) disconnecting any instrument electrical plug or other electrical connection, (3) connecting a test substitute in parallel with an electrolytic capacitor in the instrument.

b. Do not defeat any plug/socket B+ voltage interlocks with which instruments covered by this service manual might be equipped.

c. Do not apply AC power to this instrument and /or any of its electrical assemblies unless all solid-state device heat sinks are correctly installed.

d. Always connect a test instrument's ground lead to the instrument chassis ground before connecting the test instrument positive lead. Always remove the test instrument ground lead last.

Note : Refer to the Safety Precautions section ground lead last.

(2) The service precautions are indicated or printed on the cabinet, chassis or components. When servicing, follow the printed or indicated service precautions and service materials.

(3) The components used in the unit have a specified flame resistance and dielectric strength.
When replacing components, use components which have the same ratings. Components ientified by shading, by(⚠) or by (⚠) in the circuit diagram are important for safety or for the characteristics of the unit. Always replace them with the exact replacement components.

(4) An insulation tube or tape is sometimes used and some components are raised above the printed wiring board for safety. The internal wiring is sometimes clamped to prevent contact with heating components. Install such elements as they were.

(5) After servicing, always check that the removed screws, components, and wiring have been installed correctly and that the portion around the serviced part has not been damaged and so on. Further, check the insulation between the blades of the attachment plug and accessible conductive parts.

1-2-2 Insulation Checking Procedure

Disconnect the attachment plug from the AC outlet and turn the power ON. Connect the insulation resistance meter (500V) to the blades of the attachment plug. The insulation resistance between each blade of the attachment plug and accessible conductive parts(see note) should be more than 1 Megohm.

Note : Accessible conductive parts include metal panels, input terminals, earphone jacks, etc.

1-3 ESD Precautions

Electrostatically Sensitive Devices (ESD)

Some semiconductor (solid state) devices can be damaged easily by static electricity.
Such components commonly are called Electrostatically Sensitive Devices(ESD). Examples of typical ESD devices are integrated circuits and some field-effect transistors and semiconductor chip components. The following techniques should be used to help reduce the incidence of component damage caused by static electricity.

(1) Immediately before handling any semiconductor component or semiconductor-equipped assembly, drain off any electrostatic charge on your body by touching a known earth ground. Alternatively, obtain and wear a commercially available discharging wrist strap device, which should be removed for potential shock reasons prior to applying power to the unit under test.

(2) After removing an electrical assembly equipped with ESD devices, place the assembly on a conductive surface such as aluminum foil, to prevent electrostatic charge buildup or exposure of the assembly.

(3) Use only a grounded-tip soldering iron to solder or unsolder ESD devices.

(4) Use only an anti-static solder removal devices. Some solder removal devices not classified as “anti-static” can generate electrical charges sufficient to damage ESD devices.

(5) Do not use freon-propelled chemicals. These can generate electrical charges sufficient to damage ESD devices.

(6) Do not remove a replacement ESD device from its protective package until immediately before your are ready to install it.(Most replacement ESD devices are packaged with leads electrically shorted together by conductive foam, aluminum foil or comparable conductive materials).

(7) Immediately before removing the protective materials from the leads of a replacement ESD device, touch the protective material to the chassis or circuit assembly into which the device will be installed.

CAUTION : Be sure no power is applied to the chassis or circuit, and observe all other safety precautions.

(8) Minimize bodily motions when handling unpackaged replacement ESD devices. (Otherwise harmless motion such as the brushing together of your clothes fabric or the lifting of your foot from a carpeted floor can generate static electricity sufficient to damage an ESD device).

1-4 Handling the optical pick-up

The laser diode in the optical pick up may suffer electrostatic breakdown because of potential static electricity from clothing and your body.

The following method is recommended.

(1) Place a conductive sheet on the work bench (The black sheet used for wrapping repair parts.)

(2) Place the set on the conductive sheet so that the chassis is grounded to the sheet.

(3) Place your hands on the conductive sheet(This gives them the same ground as the sheet.)

(4) Remove the optical pick up block

(5) Perform work on top of the conductive sheet. Be careful not to let your clothes or any other static sources to touch the unit.

- Be sure to put on a wrist strap grounded to the sheet.
- Be sure to lay a conductive sheet made of copper etc. Which is grounded to the table.

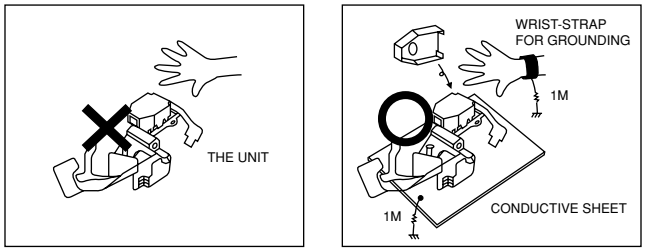


Fig.1-3

(6) Short the short terminal on the PCB, which is inside the Pick-Up ASS'Y, before replacing the Pick-Up. (The short terminal is shorted when the Pick-Up Ass'y is being lifted or moved.)

(7) After replacing the Pick-up, open the short terminal on the PCB.

1-5 Pick-up disassembly and reassembly

1-5-1 Disassembly

1) Remove the power cable.
2) Switch SW3 on deck PCB to“OFF” before removing the FPC.
   (Inserted into Main PCB DCN1. See Fig. 1-4)
3) Disassemble the deck.
4) Disassemble the deck PCB.

1-5-2 Assembly

1) Replace the Pick-up.
2) Assemble the deck PCB.
3) Reassemble the deck.
4) Insert FPC into Main PCB DCN1 and switch SW3 on deck PCB to “ON”. (See Fig 1-4)

Note : If the assembly and disassembly are not done in correct sequence, the Pick-up may be damaged.

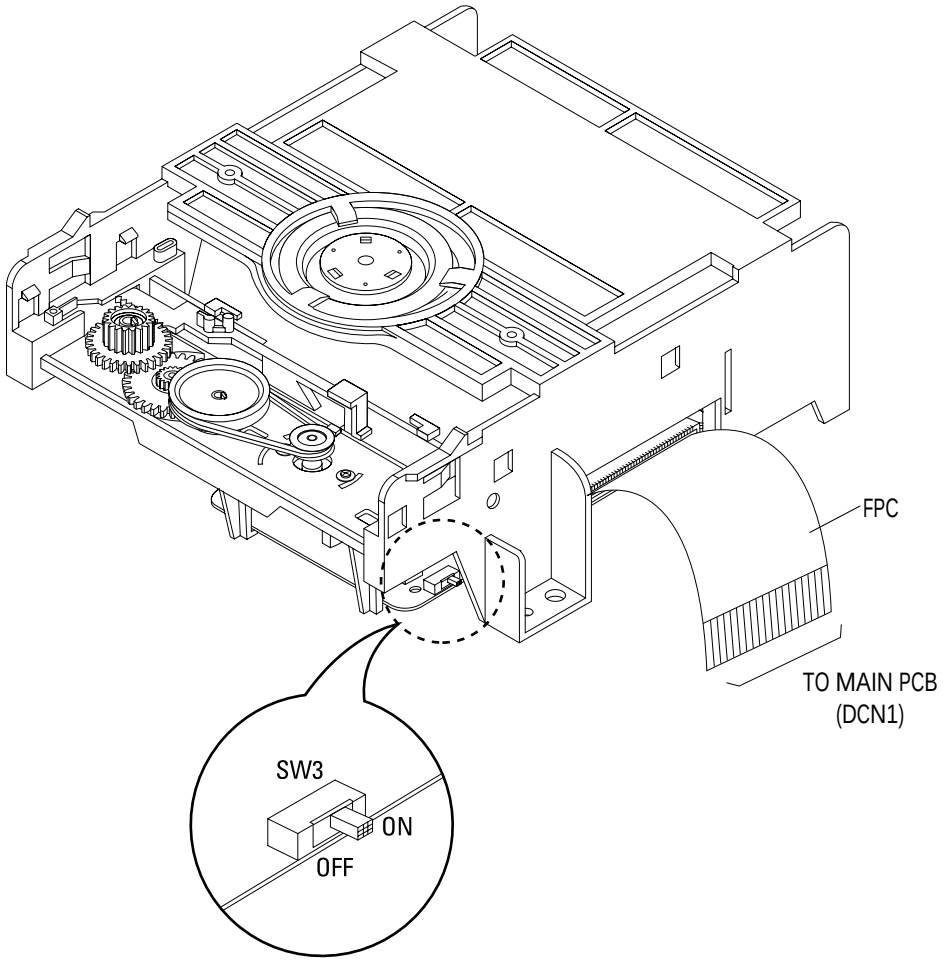
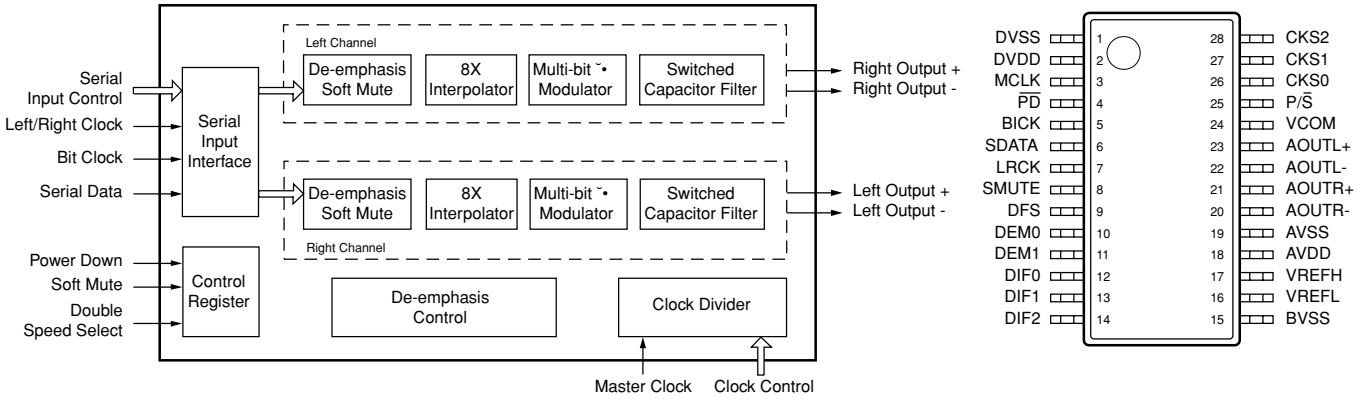


Fig. 1-4

2. Reference Information

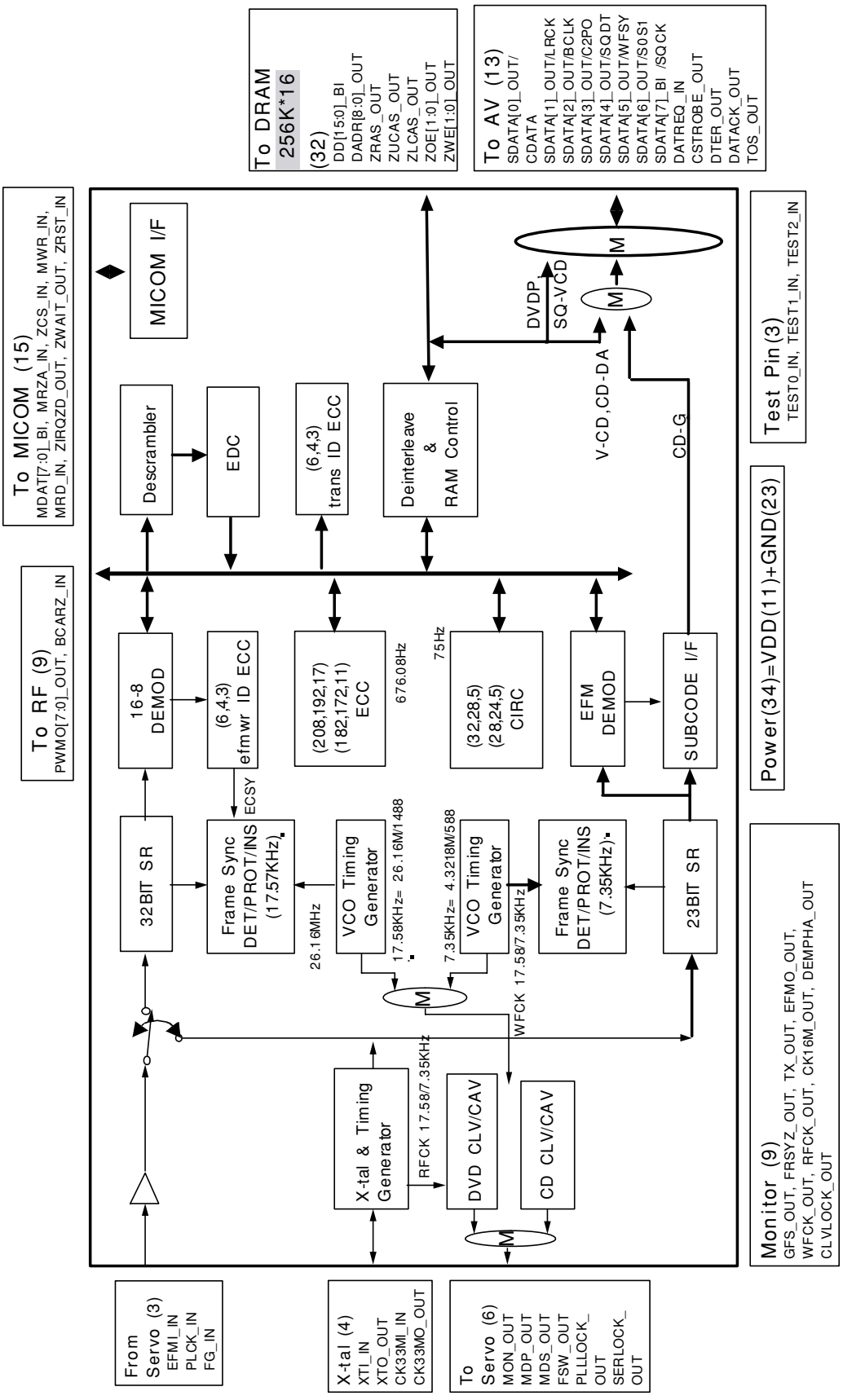
2-1 IC Dsecriptions

2-1-1 AIC1 (AK4393 ; Digital-to-Analog Converter)



No.	Pin Name	I/O	Pin Function and Description
1	DVSS	-	Digital Ground. Digital ground is 0V.
2	DVDD	-	Digital Supply. 3.3V or 5.0V nominal.
3	MCLK	I	Master Clock Input.
4	PD	I	Power-down and Reset. When low the AK4393 is in Power-down Mode and held in reset. The AK4393 should always be reset after power-up.
5	BICK	I	Audio Serial Data Clock Input. A clock input of 64fs or more is recommended.
6	SDATA	I	Serial Data Input.
7	LRCK	I	Left/Right Clock Input. Defines the sampling rate, F_s.
8	SMUTE (or $\overline{CS}$)	I	Soft Mute Input or Chip Select Input. If the P/$\overline{S}$ pin (pin 25) is high, SMUTE controls the soft mute function as follows: - When SMUTE goes high, the soft mute cycle is initiated. - When SMUTE goes low, the output mute is slowly released. If the P/$\overline{S}$ pin is low, SMUTE is the Chip Select Input for the Serial Control Mode. Chip select is active when SMUTE is low.
9	DFS	I	Double Sampling Speed Input. When low, this pin defines the Normal Speed Mode, and 128 xF_s oversampling is implemented. When high, the DFS pin defines the Double Speed Mode, implemented with 64 x F_s oversampling. This pin features an internal pull-down.
10	DEM0 (or CCLK)	I	De-emphasis Enable #0 or Control Data Clock Input. If the P/$\overline{S}$ pin (pin 25) is high, DEM0 is used to select the De-emphasis Mode according to Table 3. If the P/$\overline{S}$ pin os low DEM0 is the clock input for the Serial Control Mode.
11	DEM1 (or CDTI)	I	De-emphasis Enable #1 or Control Data Input. If the P/$\overline{S}$ pin (pin 25) is high, DEM1 is used to select the De-emphasis Mode according to Table 3. If the P/$\overline{S}$ pin is low, DEM1 is the control data input for the Serial Control Mode.
12	DIF0	I	Digital Input Format Select #0.
13	DIF1	I	Digital Input Format Select #1.
14	DIF2	I	Digital Input Format Select #2.
15	BVSS	-	Substrate Ground Pin. Substrate ground is 0V.
16	VREFL	I	Low Level Voltage Reference Input. Normally connected to analog ground.
17	VREFH	I	High Level Voltage Reference Input. Normally connected to analog supply.
18	AVDD	-	Analog Supply. Analog supply is 5V nominal.
19	AVSS	-	Analog Ground. Analog ground is 0V.
20	AOUTR-	O	Right Channel Negative Output.
21	AOUTR+	O	Right Channel Positive Output.
22	AOUTL-	O	Left Channel Negative Output.
23	AOUTL+	O	Left Channel Positive Output.
24	VCOM	O	Common Voltage Output. Common voltage output is 2.6V nominal.
25	P/$\overline{S}$	I	Parallel/Serial Control Mode Select Input. If Low, the Serial Control Mode is implemented. If High, the Parallel Control Mode is selected. This pin has an internal pull-up.
26	CKS0	I	Master Clock Select #0.
27	CKS1	I	Master Clock Select #1.
28	CKS2	I	Master Clock Select #2.

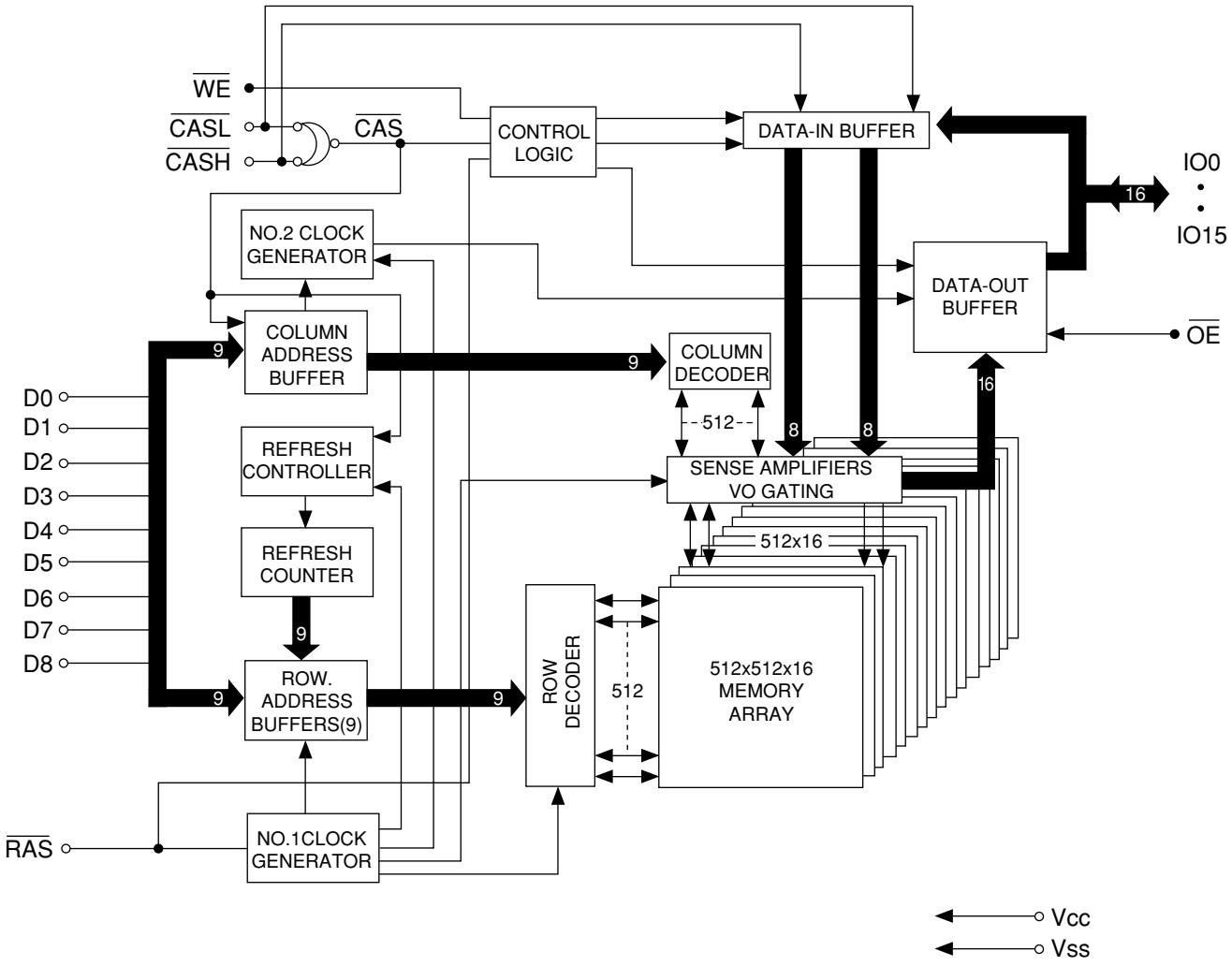
2-1-2 DIC1 (KS1453 ; Data Processor)



No.	Pin Name	Description	I/O	Notes
1	DVSS	Digital GND (0 V)		
2	ZCS_IN	Chip Select (Active Low)	I	MICOM
3	MRZA_IN	Micom Register Select (L REGISTER H fi DATA)	I	MICOM
4	DVSS	Digital GND (0 V)		
5	MDAT7_BI	MICOM Data Bus	B	MICOM
6	MDAT6_BI	MICOM Data Bus	B	MICOM
7	MDAT5_BI	MICOM Data Bus	B	MICOM
8	MDAT4_BI	MICOM Data Bus	B	MICOM
9	MDAT3_BI	MICOM Data Bus	B	MICOM
10	MDAT2_BI	MICOM Data Bus	B	MICOM
11	MDAT1_BI	MICOM Data Bus	B	MICOM
12	MDAT0_BI	MICOM Data Bus	B	MICOM
13	DVDD	Digital Power (+5V)		
14	XTI_IN	System Clock Input for 26.16 MHz	I	XTAL
15	XTO_OUT	System Clock Output for 26.16 MHz	O	XTAL
16	DVSS	Digital GND (0 V)		
17	DD15_BI	DRAM Data Bus	B	DRAM
18	DD0_BI	DRAM Data Bus	B	DRAM
19	DD14_BI	DRAM Data Bus	B	DRAM
20	DD1_BI	DRAM Data Bus	B	DRAM
21	DVSS	Digital GND (0 V)		
22	DD13_BI	DRAM Data Bus DRAM Address Bus	B	DRAM
23	DD2_BI	DRAM Data Bus	B	DRAM
24	DD12_BI	DRAM Data Bus	B	DRAM
25	DD3_BI	DRAM Data Bus	B	DRAM
26	DVDD	Digital Power (+5 V)		
27	DD11_BI	Digital Data Bus	B	DRAM
28	DD4_BI	Digital Data Bus	B	DRAM
29	DD10_BI	Digital Data Bus	B	DRAM
30	DD5_BI	Digital Data Bus	B	DRAM
31	DVSS	Digital GND (0 V)		
32	DD9_BI	DRAM Data Bus	B	DRAM
33	DD6_BI	DRAM Data Bus	B	DRAM
34	DD8_BI	DRAM Data Bus	B	DRAM
35	DD7_BI	DRAM Data Bus	B	DRAM
36	DVSS	Digital GND (0 V)		
37	ZLCAS_OUT	DRAM Low Column Address Strobe	O	DRAM
38	ZUCAS_OUT	DRAM Upper Column Address Strobe	O	DRAM
39	ZWE1_OUT	DRAM Write Enable 1 (8M ONLY)	O	DRAM
40	ZWE0_OUT	DRAM Write Enable 0 (4M, 8M, 16M)	O	DRAM
41	ZOE1_OUT	DRAM Output Enable 1 (16M MODE DADR9)	O	DRAM
42	DVDD	Digital Power (+5 V)		
43	ZOE0_OUT	DRAM Output Enable 0	O	DRAM
44	ZRAS_OUT	DRAM Row Address Strobe	O	DRAM
45	DADR8_OUT		O	DRAM
46	DADR7_OUT	DRAM Address Bus	O	DRAM
47	DVSS	Digital GND (0 V)		
48	DADR0_OUT	DRAM Address Bus	O	DRAM
49	DADR6_OUT	DRAM Address Bus	O	DRAM
50	DADR1_OUT	DRAM Address Bus	O	DRAM
51	DADR5_OUT	DRAM Address Bus	O	DRAM
52	DADR2_OUT	DRAM Address Bus	O	DRAM
53	DADR4_OUT	DRAM Address Bus	O	DRAM
54	DADR3_OUT	DRAM Address Bus	O	DRAM
55	DVSS	Digital GND (0 V)		
56	DVSS	Digital GND (0 V)		
57	TOS_OUT	Top of Sector	O	AV Decoder
58	DATACK_OUT	Data Acknowledge Signal Output	O	AV Decoder
59	DVDD	DIGITAL Power (+5 V)		
60	SDATA0_OUT	DVD Data/CD Data Bit Stream (CDATA)	O	AV Decoder
61	SDATA1_OUT	DVD Data/CD Data L/R Clock (LRCK)	O	AV Decoder
62	SDATA2_OUT	DVD Data/CD Data Bit Clock (BLCK)	O	AV Decoder
63	SDATA3_OUT	DVD Data/CD Data Error Flag (C2PO)	O	AV Decoder
64	SDATA4_OUT	DVD Data/Subcode Serial Data (SQDT)	O	AV Decoder

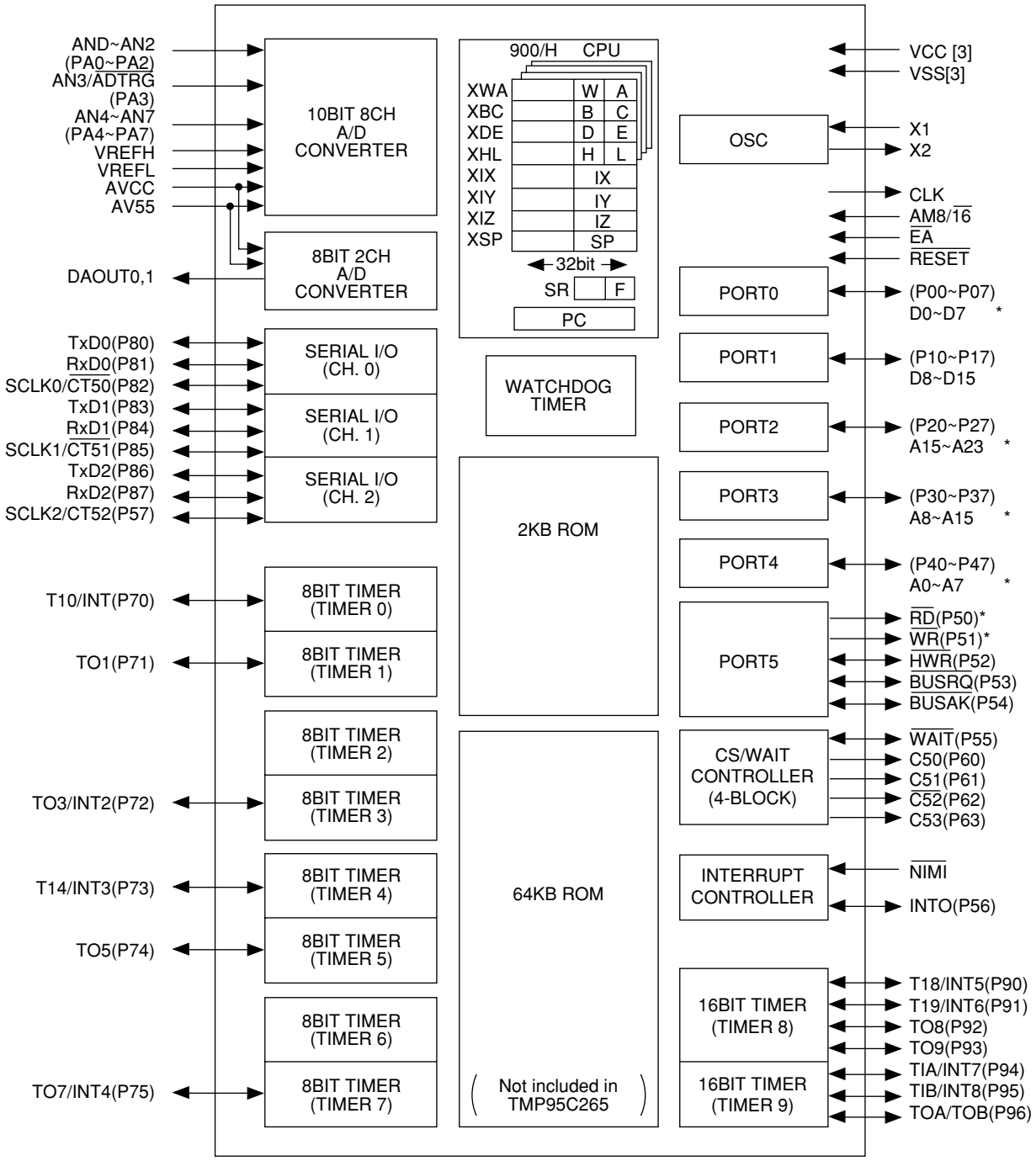
No.	Pin Name	Description	I/O	Notes
65	SDATA5_OUT	DVD Data/Subcode Frame Sync (WFSY)	O	AV Decoder
66	SDATA6_OUT	DVD Data/Subcode Block Sync (S0S1)	O	AV Decoder
67	SDATA7_BI	DVD Data/Subcode Serial Clock (SQCK)	B	AV Decoder
68	DVSS	Digital GND (0 V)		
69	CSTROBE_OUT	Data Strobe (Clock) Output	O	AV Decoder
70	DATREQ_IN	Data Request from A/V Decoder or ROM Decoder	I	AV Decoder
71	DTER_OUT	DVD Data Error Output	O	AV Decoder
72	DVSS	Digital GND (0 V)		
73	PWMO7_OUT	PWM Output Signal	O	RF
74	PWMO6_OUT	PWM Output Signal	O	RF
75	PWMO5_OUT	PWM Output Signal	O	RF
76	PWMO4_OUT	PWM Output Signal	O	RF
77	DVDD	Digital Power (+5 V)		
78	PWMO3_OUT	PWM Output Signal	O	RF
79	PWMO2_OUT	PWM Output Signal	O	RF
80	PWMO1_OUT	PWM Output Signal	O	RF
81	PWMO0_OUT	PWM Output Signal	O	RF
82	DVSS	Digital GND (0 V)		
83	DVSS	Digital GND (0 V)		
84	DVSS	Digital GND (0 V)		
85	DVDD	DIGITAL Power (+5 V)		
86	DVDD	DIGITAL Power (+5 V)		
87	DVSS	Digital GND (0 V)		
88	DVSS	Digital GND (0 V)		
89	DVSS	Digital GND (0 V)		
90	DVSS	Digital GND (0 V)		
91	FRSYZ_OUT	Frame Sync Out	O	Monitor
92	TX_OUT	Digital Out	O	Monitor
93	GFS_OUT	Good Frame Sync Detection State Output (OK at H)	O	Monitor
94	DVSS	Digital GND (0 V)		
95	CK33MI_IN	System Clock Input for 33.8688 MHz	I	X-tal
96	CK33MO_OUT	System Clock Output for 33.8688 MHz	O	X-tal
97	DVDD	Digital Power (+5 V)		
98	TEST0_IN	Test Mode Selection Terminal	I	
99	TEST1_IN	Test Mode Selection Terminal	I	
100	TEST2_IN	Test Mode Selection Terminal	I	
101	EFMO_OUT	EFM Out	O	Monitor
102	WFCK_OUT	Write Frame Pulse	O	Monitor
103	RFCK_OUT	Reference Frame Pulse	O	Monitor
104	PLCK_IN	Phase Locked Clock	I	Servo
105	DVSS	Digital GND (0 V)		
106	PLLLOCK_OUT	Lock Signal for PLL	O	Servo
107	CLVLOCK_OUT	Lock Signal for CLV	O	Monitor
108	SERLOCK_OUT	Lock Signal for SERVO	O	Servo
109	MDP_OUT	Spindle Motor Phase Control Signal (3-STATE)	O	Servo
110	MDS_OUT	Spindle Motor Speed Control Signal (3-STATE)	O	Servo
111	DVSS	Digital GND (0 V)		
112	DVSS	Digital GND (0 V)		
113	MON_OUT	Spindle Motor Output Filter Switching Output	O	Servo
114	FG_IN	Reference Signal for CAV	I	Servo
115	FSW_OUT	Spindle Motor Output Filter Switching Output (3-STATE)	O	Servo
116	EFMI_IN	EFM/EFM+ Signal Input Notes	I	Servo
117	DVDD	Digital Power (+5 V)		
118	DVDD	Digital Power (+5 V)		
119	DVDD	Digital Power (+5 V)		
120	CK16M_OUT	CK33Ms 2 Division Clock / 16.9344 MHz	O	Monitor
121	DEMPHA_OUT	HIGH, when on Deemphasis	O	Monitor
122	BCARZ_IN	BCA Input Signal	I	RF
123	DVSS	Digital GND (0 V)		
124	ZRST_IN	Hardware Reset (Active Low)	I	MICOM
125	ZWAIT_OUT	Micom Read / Write Access Wait (Wait at L)	O	MICOM
126	ZIRQZD_OUT	Interrupt Request to Micom	O	MICOM
127	MRD_IN	Micom Read Strobe (Active Low)	I	MICOM
128	MWR_IN	Micom Write Strobe (Active Low)	I	MICOM

2-1-3 DIC2 (KM416C254D ; CMOS 4M DRAM)



PIN NO.	SYM.	TYPE	DESCRITION
16~19, 22~26	A0~A8	Input	Address Input
14	$\overline{RAS}$	Input	Row Address Strobe
28	$\overline{CASH}$	Input	Column Address Strobe/Upper Byte Control
29	$\overline{CASL}$	Input	Column Address Strobe/Lower Byte Control
13	$\overline{WE}$	Input	Write Enable
27	$\overline{OE}$	Input	Output Enable
2~5, 7~10, 31~34, 36~39	I/O0~I/O15	Input/Output	Data Input/Output
1, 6, 20	Vcc	Supply	Power, 5V
21, 35, 40	Vss	Ground	Ground
11, 12, 15, 30	NC	-	No Connect

2-1-4 MIC1 (TMP95C265 ; Main Micom)

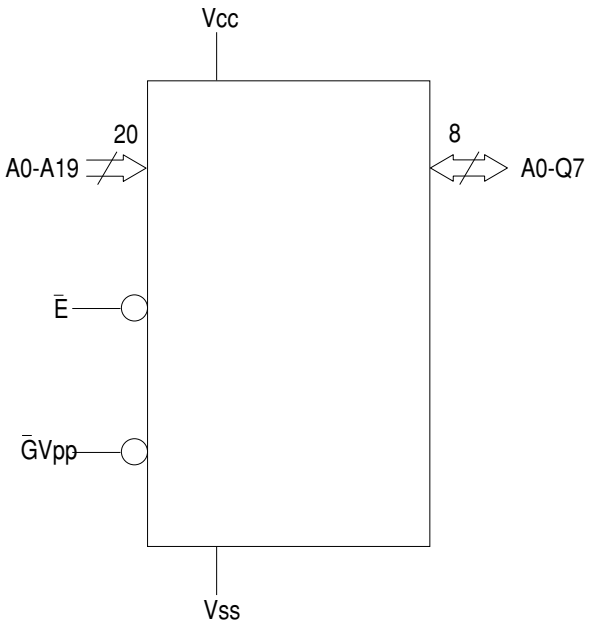


NO	PORT NAME	ASSIGNED NAME	DESCRIPTION	TYPE	REMARK
1	VREFL	DGND	A/D Ref Input(L)	I	DGND
2	AVss	DGND	A/D Ref Input	-	DGND
3	AVcc	5D	A/D VCC Input	-	5D
4	DAOUT0	MTP1		0	NC
5	DAOUT1	MPT2		0	NC
6	/NMI	-	PULL-UP	I	
7	P53	CSB	D. Servo IC Chip Select	0	KS1452(10)
8	P54/BUSAK	MTP3		0	
9	/WAIT	/MWAIT	/Wait(ZiVA, DSP)	I	/MWait
10	P56	DVD/CD	DVD/CD RF AGC Gain Select	0	RF(KS1461)
11	SCLK2	SCLK	Serial Data Clock	I	FRONT
12	P80/TXD0	MD	RF Contrl Data	0	KS1461(69)
13	P81/RXD0	STB	RF Data Latch	I/0	KS1461(71)
14	P82/SCLKO	MC	RF Control Clock	0	KS1461(70)
15	P83/TXD1	MTP5		0	NC
16	P84/RXD1	MTP6		0	NC
17	P85/SCLK1	MTP4		0	NC
18	TXD2	RXD	Serial Data Output	0	FRONT
19	RXD2	TXD	Serial Data Input	I	FRONT
20	CSO	/CSO	EPROM(M27C801) Select	0	EPROM(M27C801)
21	CS1	/CS1	SRAM(KM681000) Select	0	SRAM(KM681000)
22	CS2	/DVD1CS	AVDecoder(ZiVA4) Select	0	AVDecoder(ZiVA4)
23	CS3	/DSPCS	Data Processor(KS1453) Select	0	Data Processor(KS1453)
24	CLK	CLK	CLOCK OUTPUT (System Clock÷2)	0	fc/2
25	Vcc	5D		-	VCC
26	Vss	GDND	GND	-	GND
27	X1	X1	High Frequency OSC in	I	20MHz
28	X2	X2	High frequency OSC out	0	
29	/EA	/EA	Internal ROM Less Mode	I	GND
30	/REST	/MRST	Master reset from FRONT	I	FRONT, IC
31	INT1	SRQ	Interrupt from Front Micom	I	FRONT
32	P71	RRQ	Request to Front Micom	0	FRONT
33	P72	SCL	EEPROM CLOCK	0	KS24C020(6)
34	P73	SDA	EEPROM DATA I/O	0	KS24C020(5)
35	P74	OPEN	Tray Out Motor Control Output	0	DRIVER(0PIN-, 16)
36	P75	CLOSE	Tray In Motor Control Output	0	DRIVER(0PIN-, 17)
37	INT5	FGINT	Interrupt from Spindle Motor FG	I	DRIVER(FG, 2)
38	P91	ACT MUTE	Driver IC MUTE(Actuator)	0	DRIVER(MUTE4, 37)
39	P92	M/D MUTE	Driver IC MUTE(Spindle)	0	DRIVER(MUTE3, 38)
40	P93	ZRST	DSP H/W reset	0	KS1453(124)
41	INT7	/DVDINT	Interrupt from AV-DEC	I	INV(ZiVA-4(51))
42	INT8	/DSPINT	Interrupt from DSP	I	INV(KS1453(126))
43	P96	ZIVA_RST	AV Decoder Reset(Active H:4.0, L:4.1)	0	ZiVA-4(52)
44	Vcc	5D			
45	D0	HAD0	Data 0	I/0	
46	D1	HAD1	Data 1	I/0	
47	D2	HAD2	Data 2	I/0	
48	D3	HAD3	Data 3	I/0	
49	D4	HAD4	Data 4	I/0	
50	D5	HAD5	Data 5	I/0	

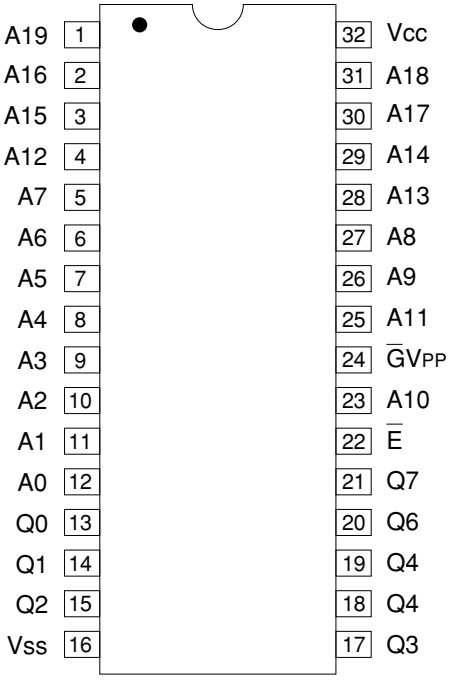
NO	PORT NAME	ASSIGNED NAME	DESCRIPTION	TYPE	REMARK
51	D6	HAD6	Data6	I/0	
52	D7	HAD7	Data7	I/0	
53	P10	CLSW	Close Switch	I	DECK
54	P11	OPSW	Open Swithc	I	DECK
55	P12	MTP8	Reserved I/0	0	NC
56	P13	MTP9	Reserved I/0	0	NC
57	P14	MTP10	Reserved I/0	0	NC
58	P15	MTP11	Reserved I/0	0	NC
59	P16	MTP12	Reserved I/0	0	NC
60	P17	MTP13	Reserved I/0	0	NC
61	AM8/16	AM8	Address Mode(H:8 BIT MODE)	I	VCC
62	Vss	DGND		-	GND
63	Vcc	5D		-	VCC
64	A23	HA23	SERVO /RD Strobe Mask Signal	0	74HCOO(5)
65	P26/A22	MRP14	Reserved Address Port	0	NC
66	P25/A21	MRP15	Reserved Address Port	0	NC
67	P24/A20	MRP16	Reserved Address Port	0	NC
68	A19	HA19	Address 19	0	EPROM, SRAM ADDRESS
69	A18	HA18	Address 18	0	EPROM, SRAM ADDRESS
70	A17	HA17	Address 17	0	EPROM, SRAM ADDRESS
71	A16	HA16	Address 16	0	EPROM, SRAM ADDRESS
72	A15	HA15	Address 15	0	EPROM, SRAM ADDRESS
73	A14	HA14	Address 14	0	EPROM, SRAM ADDRESS
74	A13	HA13	Address 13	0	EPROM, SRAM ADDRESS
75	A12	HA12	Address 12	0	EPROM, SRAM ADDRESS
76	A11	HA11	Address 11	0	EPROM, SRAM ADDRESS
77	A10	HA10	Address 10	0	EPROM, SRAM, Zlva Adrs
78	A9	HA9	Address 9	0	EPROM, SRAM, Zlva Adrs
79	A8	HA8	Address 8	0	EPROM, SRAM, Zlva Adrs
80	A7	HA7	Address 7	0	EPROM, SRAM ADDRESS
81	A6	HA6	Address 6	0	EPROM, SRAM ADDRESS
82	A5	HA5	Address 5	0	EPROM, SRAM ADDRESS
83	A4	HA4	Address 4	0	EPROM, SRAM ADDRESS
84	A3	HA3	Address 3	0	EPROM, SRAM ADDRESS
85	A2	HA2	Address 2	0	EPROM, SRAM ADDRESS
86	A1	HA1	Address 1(SERVO DAB)	0	EPROM, SRAM ADDRESS
87	A0	HA0	Address 0(DSP DAB)	0	EPROM, SRAM ADDRESS
88	/RD	/RD	/Read Strobe	0	/Read
89	/WR	/WR	/Write Strobe	0	/Write
90	P52	RSTB	RF&Servo IC Reset	0	KS1461 (73), KS1452 (9)
91	Vss	DGND		-	DGND
92	PA0	RFRP	Tracking Lock monitir from SERVO	I	KS1452 (7)
93	PA1	TILTO	Monitor signal	I	KS1452 (69)
94	PA2	MTP17	Reserved I	I	NC
95	PA3	SENSE	SENSE monitor from SERVO	I	KS1452 (22)
96	PA4	FR	Spindle direcrion from SP Driver	I	BA6849FP (20)
97	PA5	SLOCK	LOCK monitor from DSP	I	KS1453 (108)
98	PA6	FOKB	Focus lock monitor from RF	I	KS1461 (48)
99	PA7	RFO	RF sum signal (Analog Lnput)	I	RFO
100	VREFH	5D	A/D Ref Input (H)	I	5D

2-1-5 MIC2 (M27C801 ; 8Mbit (1Mbx8) UVEPROM and OTP EPROM)

LOGIC DIAGRAM



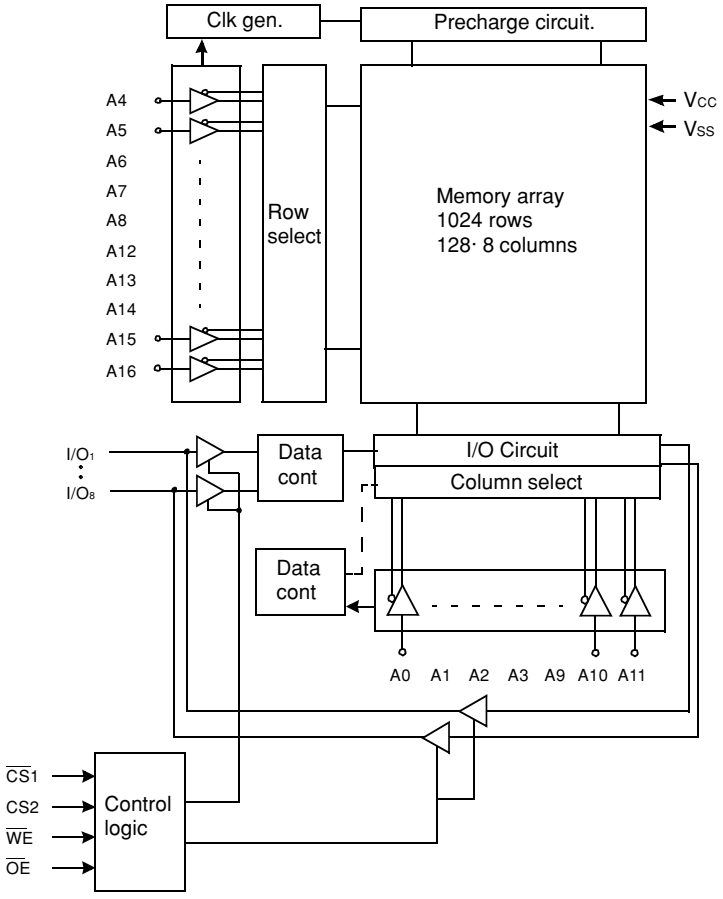
TOP VIEW



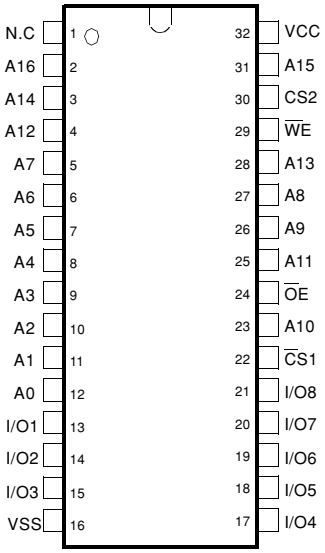
NAME	FUNCTION
A0-A19	Address Inputs
Q0-Q7	Data Outputs
Ē	Chip Enable
ŌVpp	Output Enable/Program Supply
Vcc	Supply Voltage
Vss	Ground

2-1-6 MIC3 (KM681000C ; CMOS 1M SRAM)

BLOCK DIAGRAM

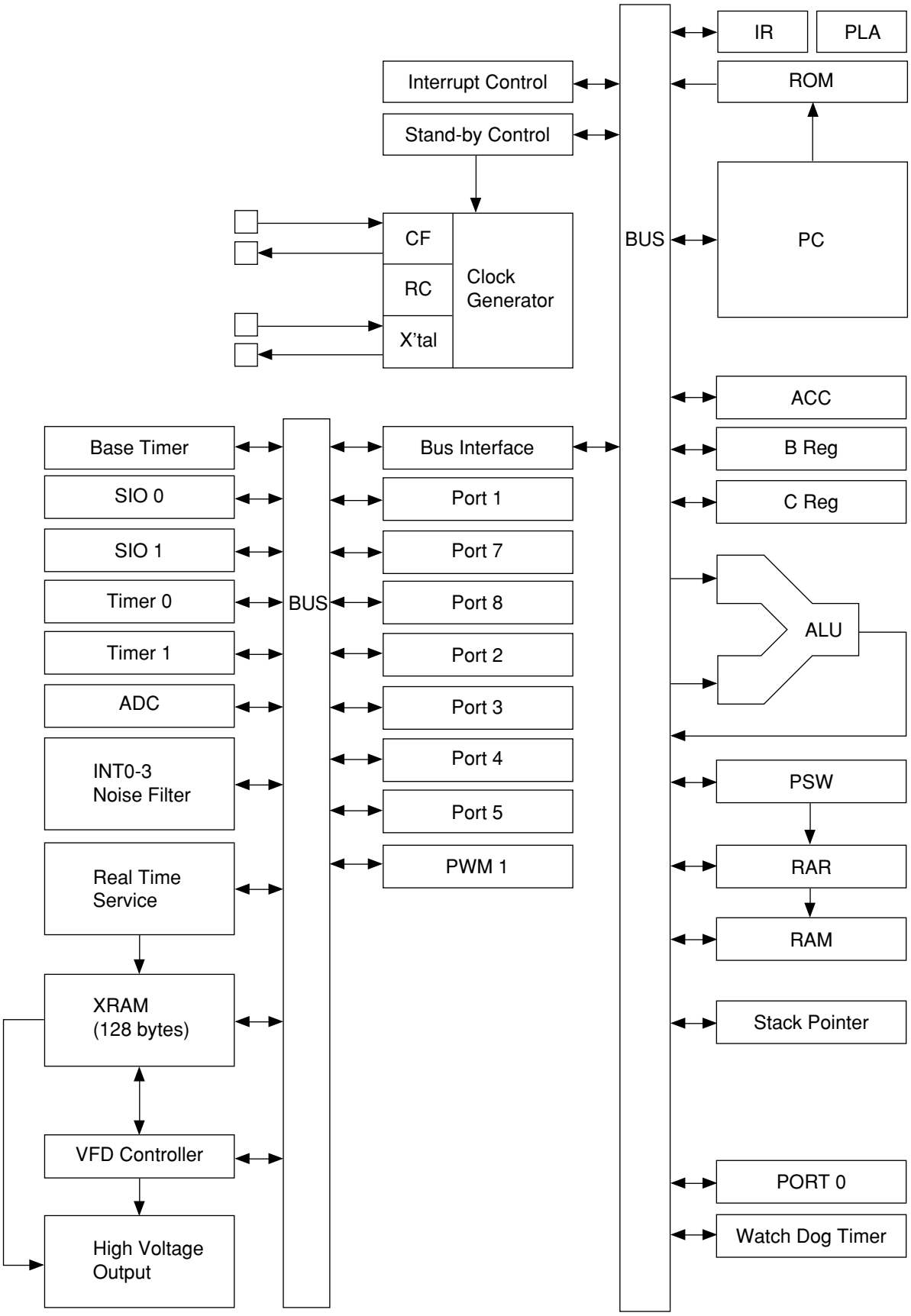


TOP VIEW



Name	Function	Name	Function
$\overline{CS}_1$,CS_2	Chip Select Inputs	I/O_1~I/O_8	Data Inputs/Out-
$\overline{OE}$	Output Enable	Vcc	Power
$\overline{WE}$	Write Enable	Vss	Ground
A_0~A_{16}	Address Inputs	N.C	No Connection

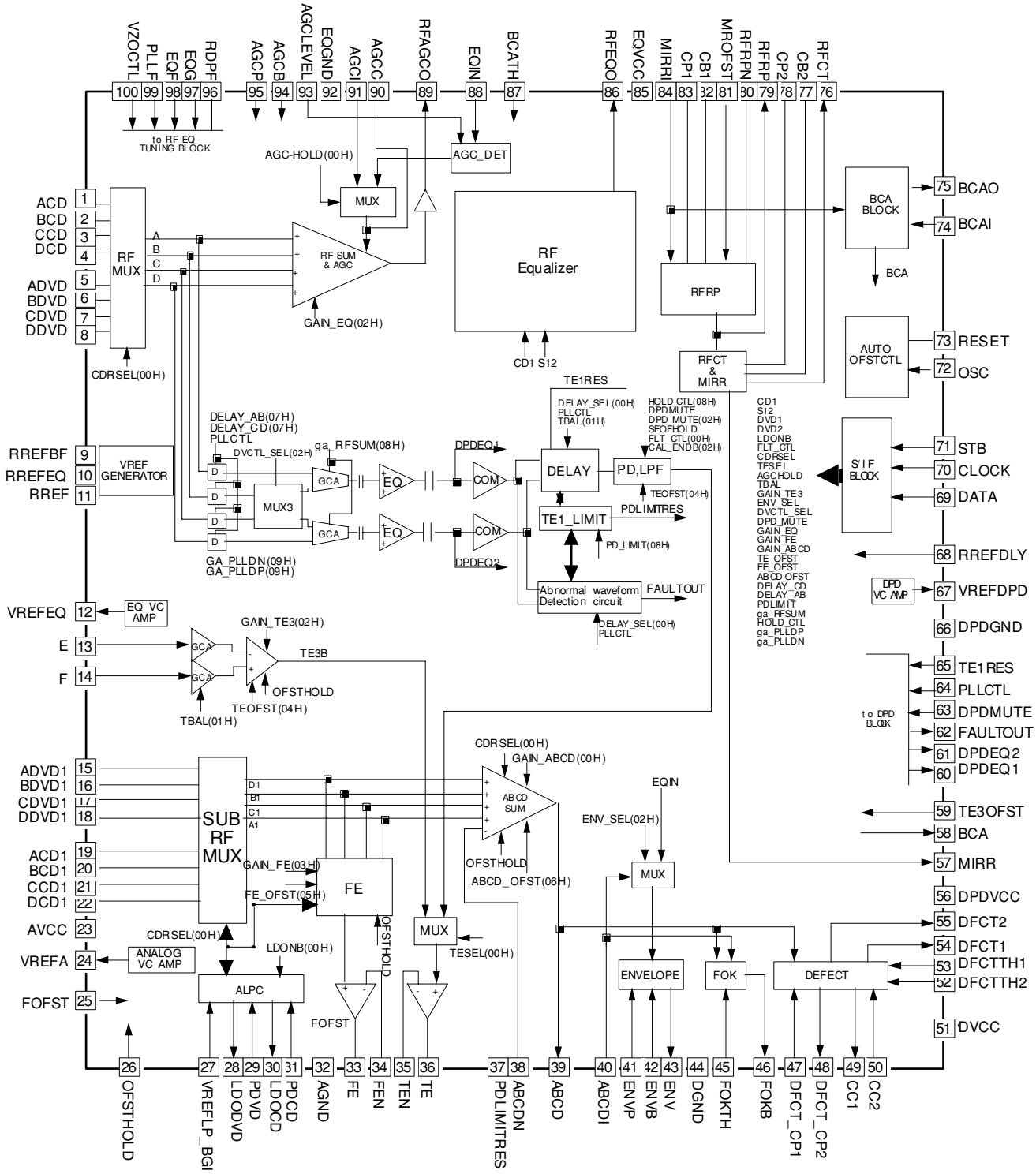
2-1-7 FIC1 (LC86P6232 ; Front Micom)



NO	PORT NAME	TYPE	ASSIGNED NAME	DESCRIPTION	REMARK
1	P52	0	MRST	Front end reset	RESET
2	PWM1	-	TP1		NC
3	P20	0	CS1	Chip Select 1	AK4393
4	P21	0	CCLK	Control Data Clock	AK4393/AK4356
5	P22	0	CDTI	Control Data	AK4393/AK4356
6	P23	0	CS2	Chip Select 2	AK4356
7	P24	0	DARST	PD(Power Down)	AK4393
8	P25	0	DARST 1	PD(Power Down)	AK4356
9	P26	0	VMUTE0	BA7660 MUTE(VIC2)	VIDEO(RESERVED)
10	P27	0	VMUTE1	BA7660 MUTE(VIC1)	VIDEO(RESERVED)
11	TEST1	-	TP4		NC
12	*RES	I	*RES	Reset	
13	XT1	-	GND	Low Frequency OSC in	
14	XT2	-	TP5	Low Frequency OSC out	
15	VSS	-	GND		
16	CF1	I	-	High Frequency OSC in	
17	CF2	0	-	High Frequency OSC out	
18	VDD	-	VDD		
19	ANO/P8 0	I	ECHO_VR	ECHO volume A/D input	KARAOKE
20	AN1/P8 1	I	MIC_DET	MIC detect	KARAOKE
21	AN2/P8 2	-	TP19		NC
22	AN3/P8 3	I	KEY0	KEY SCAN	TACT SW
23	AN4/P8 4	I	KEY1	KEY SCAN	TACT SW
24	AN5/P8 5	I	KEY2	KEY SCAN	TACT SW
25	AN6/P8 6	-	NC		
26	AN7/P8 7	-	NC		
27	P70/IN TO	I	RRQ	Request to Front Micom	MAIN MICOM
28	P71/IN T1	-	TP25		NC
29	P72/IN T2	-	TP26		NC
30	P73/IN T3	I	REMOCON	REMOCON data in	REMOCON EYE
31	S0/T0	0	GRID11	FLT GRID CONTROL	FLT
32	S1/T1	0	GRID10	FLT GRID CONTROL	FLT
33	S2/T2	0	GRID9	FLT GRID CONTROL	FLT
34	S3/T3	0	GRID8	FLT GRID CONTROL	FLT
35	S4/T4	0	GRID7	FLT GRID CONTROL	FLT
36	S5/T5	0	GRID6	FLT GRID CONTROL	FLT
37	S6/T6	0	GRID5	FLT GRID CONTROL	FLT
38	S7/T7	0	GRID4	FLT GRID CONTROL	FLT
39	S8/T8	0	GRID3	FLT GRID CONTROL	FLT
40	S9/T9	0	GRID2	FLT GRID CONTROL	FLT
41	S10/T10	0	GRID1	FLT GRID CONTROL	FLT
42	S11/T11	0			
43	S12/T12	0	SEG1	FLT SEGMENT CONTROL	FLT
44	S13/T13	0	SEG2	FLT SEGMENT CONTROL	FLT
45	S14/T14	0	SEG3	FLT SEGMENT CONTROL	FLT
46	S15/T15	0	SEG4	FLT SEGMENT CONTROL	FLT
47	VOD	-	+5V		
48	VP	-	-28V		
49	S16	0	SEG5	FLT SEGMENT CONTROL	FLT
50	S17	0	SEG6	FLT SEGMENT CONTROL	FLT

NO	PORT NAME	TYPE	ASSIGNED NAME	DESCRIPTION	REMARK
51	S18	-	SEG7	FLT SEGMENT CONTROL	FLT
52	S19	-	SEG8	FLT SEGMENT CONTROL	FLT
53	S20	-	SEG9	FLT SEGMENT CONTROL	FLT
54	S21	0	SEG10	FLT SEGMENT CONTROL	FLT
55	S22	0	SEG11	FLT SEGMENT CONTROL	FLT
56	S23	0	SEG12	FLT SEGMENT CONTROL	FLT
57	S24	0	SEG13	FLT SEGMENT CONTROL	FLT
58	S25	0	SEG14	FLT SEGMENT CONTROL	FLT
59	S26	0	SEG15	FLT SEGMENT CONTROL	FLT
60	S27	0	SEG16	FLT SEGMENT CONTROL	FLT
61	S28	0	SEG17	FLT SEGMENT CONTROL	FLT
62	S29	0	SEG18	FLT SEGMENT CONTROL	FLT
63	S30	0	SEG19	FLT SEGMENT CONTROL	FLT
64	S31	0	SEG20	FLT SEGMENT CONTROL	FLT
65	P00	I	MODE4	HARDWARE MODE SELECT	MARKET CODE
66	P01	I	MODE3	HARDWARE MODE SELECT	MARKET CODE
67	P02	I	MODE2	HARDWARE MODE SELECT	MARKET CODE
68	P03	I	MODE1	HARDWARE MODE SELECT	MARKET CODE
69	P04	I	MODE0	HARDWARE MODE SELECT	MARKET CODE
70	P05	-	TP10		NC
71	P06	-	TP11		NC
72	P07	--			NC
73	P10/S0 0	0	TXD	SERIAL DATA OUT	SERIAL DATA OUT
74	P11/S1 0	I	RXD	SERIAL DATA IN	SERIAL DATA IN
75	P12/SC K0	0	SCLK	SERIAL CLOCK	SERIAL CLOCK
76	P13/S0 1	-	TP12		NC
77	P14/SI 1	-	TP13		NC
78	P15/SC K1	-	TP14		NC
79	P16/BU Z	-	TP15		NC
80	P17/PW MO	-	TP16		NC
81	P30	I	S1	SHUTTLE DATA	JOG/SHUTTLE
82	P31	I	S2	SHUTTLE DATA	JOG/SHUTTLE
83	P32	I	S3	SHUTTLE DATA	JOG/SHUTTLE
84	P33	I	S4	SHUTTLE DATA	JOG/SHUTTLE
85	P34	I	J1	JOG DATA	JOG/SHUTTLE
86	P35	I	J2	JOG DATA	JOG/SHUTTLE
87	P36	I	AT	VIDEO OUT SEL.	VIDEO SELECT(OPEN)
88	P37	I	AD	VIDEO OUT SEL.	VIDEO SELECT
89	VSS	-	+5V		
90	VDD	-	GND		
91	P40	0	RGBCTL	SCART CONTROL	SCART JACK
92	P41	0	SCON_B	SCART CONTROL	SCART JACK
93	P42	-	TP28		NC
94	P43	0	WIDE	SCART CONTROL	SCART JACK
95	P44	0	SRQ	request to main micom	NC
96	P45	0	SAVE	POWER SAVE MODE	POWER
97	P46	0	AMUTE1	REAR MUTE	AUDIO
98	P47	0	AMUTE0	FRONT MUTE	AUDIO
99	P50	0	LED	STANDBY LED	LED
100	P51	0	ON/OFF	POWER ON/OFF CONTROL	POWER

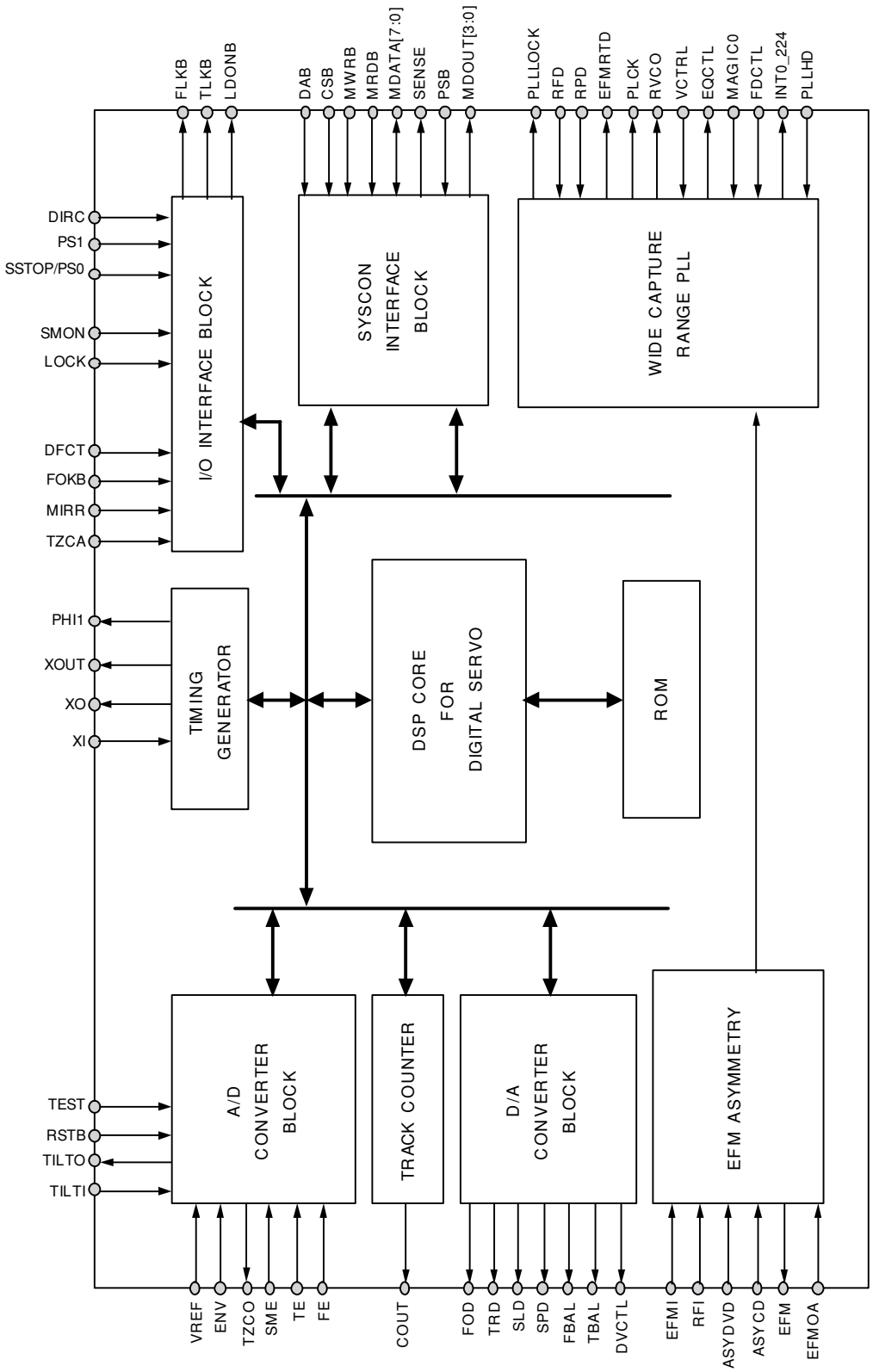
2-1-8 RIC1 (KS1461 ; RF Signal Processor)



Pin No.	Pin Name	I/O	Description	Related Block	Related Part
1	ACD	I	Optical main beam A, AC Coupling input terminals for CD of RF block	PRE AMP	P/U
2	BCD	I	Optical main beam B, AC Coupling input terminals for CD of RF block	PRE AMP	P/U
3	CCD	I	Optical main beam C, AC Coupling input terminals for CD of RF block	PRE AMP	P/U
4	DCD	I	Optical main beam D, AC Coupling input terminals for CD of RF block	PRE AMP	P/U
5	ADVD	I	Optical main beam A, AC Coupling input terminals for DVD of RF block	PRE AMP	P/U
6	BDVD	I	Optical main beam B, AC Coupling input terminals for DVD of RF block	PRE AMP	P/U
7	CDVD	I	Optical main beam C, AC Coupling input terminals for DVD of RF block	PRE AMP	P/U
8	DDVD	I	Optical main beam D, AC Coupling input terminals for DVD of RF block	PRE AMP	P/U
9	RREFBF	-	RF AMP I/O buffer bias resistance connection terminal	RF AMP	-
10	RREFEQ	-	RF EQ BIAS resistance connection terminal	RF EQ	-
11	RREF	-	Analog Block bias resistance connection terminal	ANALOG	-
12	VREFEQ	-	CAP connection terminal for RF EQ Center voltage	EQ VC AMP	-
13	E	I	CD Optical sub beam E input terminal for Servos	TE 3B	P/U
14	F	I	CD Optical sub beam F input terminal for Servos	TE 3B	P/U
15	ADVD1	I	Optical main beam A input terminal for DVD of Servo block	SERVO AMP	P/U
16	BDVD1	I	Optical main beam B input terminal for DVD of Servo block	SERVO AMP	P/U
17	CDVD1	I	Optical main beam C input terminal for DVD of Servo block	SERVO AMP	P/U
18	DDVD1	I	Optical main beam D input terminal for DVD of Servo block	SERVO AMP	P/U
19	ACD1	I	Optical main beam A input terminal for CD of Servo block	SERVO AMP	P/U
20	BCD1	I	Optical main beam B input terminal for CD of Servo block	SERVO AMP	P/U
21	CCD1	I	Optical main beam C input terminal for CD of Servo block	SERVO AMP	P/U
22	DCD1	I	Optical main beam D input terminal for CD of Servo block	SERVO AMP	P/U
23	AVCC	P	Power voltage input terminal for Analog Part	ANALOG	-
24	VREFA	I/O	CAP connection terminal for Analog Part center voltage Uses an external block	ANA VC AMP	SERVO
25	FOFST	-	CAP connection terminal (open) for Focus Auto Offsets	FE AMP	-
26	OFSTHOLD	I	On/Off terminal for Auto Offset Block. (L: Auto Offset Adjustments, H: Serial Offset Adjustments)	OFSTCTL	MICOM
27	VREFLP_BGI	I	Band gap voltage input block for ALPC	ALPC	-
28	LDODVD	O	Optical Laser Diodes operation voltage output terminal for DVD	ALPC	P/U
29	PDDVD	I	Optical Laser Monitor Diode voltage input terminal for DVD	ALPC	P/U
30	LDOCD	O	Optical Laser Diode operating voltage output terminal for CD	ALPC	P/U
31	PDCD	I	Optical Laser Monitor Diode voltage input terminal for CD	ALPC	P/U
32	AGND	P	Power GND terminal for Analog Part	ANALOG	-
33	FE	O	FE AMP output terminal	FE AMP	DSSP
34	FEN	I	Input terminal for selecting FE AMP Gain	FE AMP	-
35	TEN	I	Input terminal for selecting TE AMP Gain	TE AMP	-
36	TE	O	TE AMP output terminal	TE AMP	DSSP
37	PDLIMTRES	-	Bias resistance terminal for PDLIMIT	DPD	-
38	ABCDN	I	ABCD AMP for selecting Gain (-) input terminal	ABCD AMP	-
39	ABCD	O	ABCD AMP output terminal	ABCD AMP	-
40	ABCDI	I	ABCD AC Coupling input terminal for servo monitor	SERVO MONIT	-
41	ENVP	-	CAP connection terminal for selecting the RC value of Peak Hold for detecting RF Envelopes	RF ENV	-
42	ENVB	-	CAP connection terminal for selecting the RC value of Bottom Hold for detecting RF Envelopes	RF ENV	-
43	ENV	O	RF Envelope Detect Output terminal	RF ENV	DSSP
44	DGND	P	Power GND input terminal for digital circuits	DIGITAL	-
45	FOKTH	I	Focus OK comparating level input terminal	FOKB	-
46	FOKB	O	Focus OK comparator output terminal (L: Focus OK)	FOKB	DSSP
47	DFCT_CP1	-	Connection terminal for RC value of Peak Hold, for selecting the maximum time for Servo signal	DFCT	-
48	DFCT_CP2	-	Connection terminal for RC value of Peak Hold, for selecting the minimum defect time for PLL	DFCT	-
49	CC1	O	Peak Hold Output terminal for selecting the minimum Defect time for Defect	DFCT	-
50	CC2	I	Peak Hold AC Coupling Input terminal for Defect	DFCT	-
51	DVCC	P	Power voltage input terminal for digital circuit	DIGITAL	-
52	DFCTTH2	-	Resistance connection terminal for selecting the Defect Comparating Level for PLL	DEFECT	-
53	DFCTTH1	-	Resistance connection terminal for selecting the Defect Comparating Level for Servo	DEFECT	-
54	DFCT1	O	Defect output terminal for Servo	DEFECT	DSSP
55	DFCT2	O	Defect output terminal for PLL	DEFECT	PLL
56	DPDVCC	P	Power voltage input terminal for DPD TE	DPD	-
57	MIRR	O	Mirror output terminal	MIRR	DSSP
58	BCA	O	BCA output terminal	BCA	DSP

Pin No.	Pin Name	I/O	Description	Related Block	Related Part
59	TE3OFST	-	Cap connection terminal (open) for 3B TE Offset	3B TE AMP	-
60	DPDEQ1	O	DPD EQ (A+C) output terminal	DPD	-
61	DPDEQ2	O	DPD EQ (B+D) output terminal	DPD	-
62	FAULTOUT	O	DPD abnormal wave form output terminal (monitor)	DPD	-
63	DPDMUTE	I	DPD TE MUTE control terminal (H: Mute)	DPD	MICOM
64	PLLCTL	I	DPD TE PLL variable input terminal	DPD	SERVO
65	TE1RES	I	DPD TE PLL variable bias resistance	DPD	-
66	DPDGND	P	Power GND input terminal for DPD TE	DPD	-
67	VREFDPD	O	CAP connection terminal for DPD TE center voltage	DPD VC AMP	-
68	RREFDLY	-	Bias resistance connection terminal for Delay Block	Delay Block	-
69	DATA	I	Data input terminal	Serial Interface	MICOM
70	CLOCK	I	Clock input terminal	Serial Interface	MICOM
71	STB	I	Data Enable input terminal	Serial Interface	MICOM
72	OSC		Input terminal for RC value of OSC, for Auto Offset Block	Auto OFSTCTL	-
73	RESET	I	Reset input terminal (L: Reset) for Auto Offset Block	Auto OFSTCTL	MICOM
74	BCAI	I	BCA Filter1	BCA	-
75	BCAO	O	BCA Filter2 Related	BCA	-
76	RFCT	O	RF Ripple Center voltage output terminal for Mirror	MIRROR	DSSP
77	CB2	-	CAP connection terminal of RC value of Bottom Hold, for RFCT generation	MIRROR	-
78	CP2	-	CAP connection terminal of RC value of Peak Hold, for RFCT generation	MIRROR	-
79	RFRP	O	RF Ripple Amp output terminal for Mirror	MIRROR	DSSP
80	RFRPN	I	Input terminal for selecting RFRP Amp gain	MIRROR	-
81	MROFST	I	RF Ripple Offset control terminal for Mirror	MRROR	-
82	CB1	-	RC connection terminal of RC value of Bottom Hold, for RFRP generation	MRROR	-
83	CP1	-	RC connection terminal of RC value of Peak Hold, for RFRP generation	MRROR	-
84	MIRRI	I	Input terminal for MIRR signal generation	MRROR	-
85	EQVCC	P	Power voltage input signal for RF EQ	RF EQ	-
86	RFEQ0	0	RF EQ output terminal	RF EQ	PLL
87	BCATH	I	BCA Comparating Level control terminal	BCA	DSP
88	EQIN	I	RFAGCO input terminal for RF EQ	RFEQ,RFENV	DSSP
89	RFAGCO	O	RF AGC AMP output terminal	RF AGC	-
90	AGCC	-	CAP connection terminal for time constant of AGC	RF AGC	-
91	AGCI	I	AGC voltage input terminal while in AGC hold	RF AGC	-
92	EQGND	P	Power GND input terminal for RF EQ	RF EQ	-
93	AGCLEVEL	I	AGC Level control voltage input terminal (3.5 V) while in AGC hold off	RF AGC	-
94	AGCB	-	RC connection terminal for RC value of Bottom Hold, for RF AGC	RF AGC	-
95	AGCP	-	RC connection terminal for RC value of Peak Hold, for RF AGC	RF AGC	-
96	RDPF	-	Bias resistance connection terminal for selecting RF EQ frequency	RF EQ	-
97	EQG	I	RF EQ Boost Gain control voltage input terminal	RF EQ	DSSP
98	EQF	I	RF EQ Peak Frequency control voltage input terminal	RF EQ	DSSP
99	PLLF	I	Wide-band PLL compatible RF EQ Peak Frequency Control terminal	RF EQ	DSSP
100	VZOCTL	I	RF EQ zero control terminal	RF EQ	DSSP

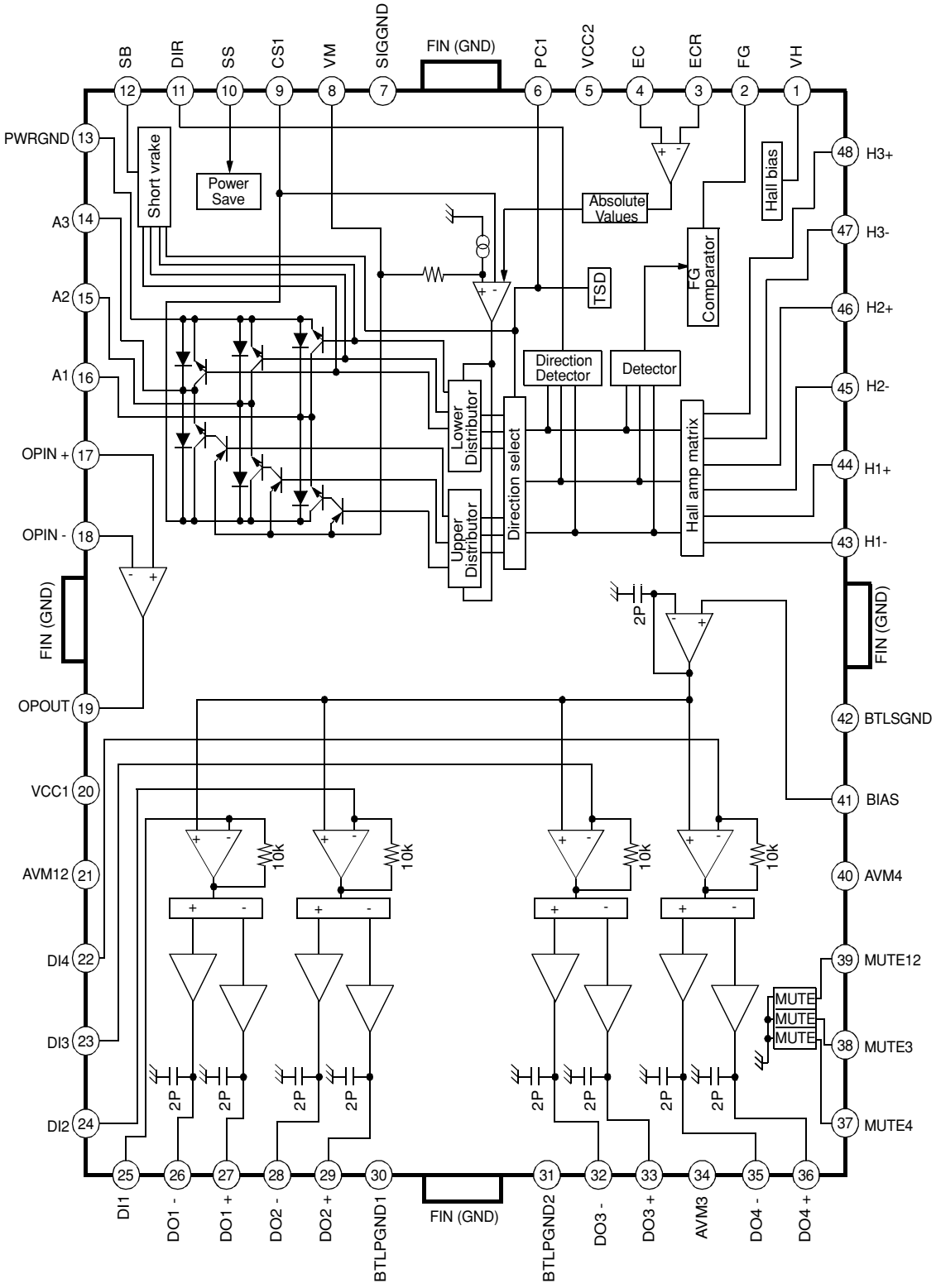
2-1-9 SIC1 (KS1452 ; Servo Processor)



No	Name	I/O	Description
1	MDOUT3	O	Mode data3 out controlled by micom
2	SSTOP/PS0PS1	I	Limit switch/sled position sensor input pin0
3	PS1	I	Sled motor position sensor input pin1
4	TEST	I	Test pin (L: normal H: test)
5	COUT	O	Counter clock
6	FLKB	O	Focus servo lock signal output pin
7	TLKB	O	Tracking servo lock signal output pin
8	PSB	I	0: 1 Bit, 1: 8 Bit
9	RSTB	I	System reset signal input pin
10	CSB	I	MICOM chip select pin
11	DAB	I	MICOM data/addrs select pin
12	MWRB	I	MICOM write clock signal input pin
13	MRDB	I	MICOM read clock signal input pin
14	MDATA0	I/O	MICOM data pin0
15	MDATA1	I/O	MICOM data pin1
16	MDATA2	I/O	MICOM data pin2
17	MDATA3	I/O	MICOM data pin3
18	MDATA4	I/O	MICOM data pin4
19	MDATA5	I/O	MICOM data pin5
20	MDATA6	I/O	MICOM data pin6
21	MDATA7	I/O	MICOM data pin7
22	SENSE	O	Internal status monitor pin
23	DVDD	P	Servo logic & ROM VDD power supply pin
24	XI	I	System clock signal input pin
25	XO	O	System clock signal output pin
26	XOUT	O	Clock out (33.9688MHz) to DSP
27	DVSS	P	Servo logic & ROM VSS power supply pin
28	SQCK	O	Clock output pin for subcode data read
29	SQSI	I	Subcode data input pin
30	SCOR	I	Timing detection input pin for subcode data read
31	SMON	I	Motor ON signal input pin
32	LOCK	I	Lock signal input pin
33	DIRC	I	Direct jump control (for 1 track jump)
34	FOKB	I	Focus OK signal input pin
35	FDCTL	I	PLL frequency detect control input pin
36	LDONB	O	Laser diode ON signal output pin
37	DFCT	I	Defect detection signal input pin
38	MIRR	I	Mirror signal input pin
39	PLLHD	I	PLL hold signal from micom
40	INT0_224	O	Servo interrupt monitor pin

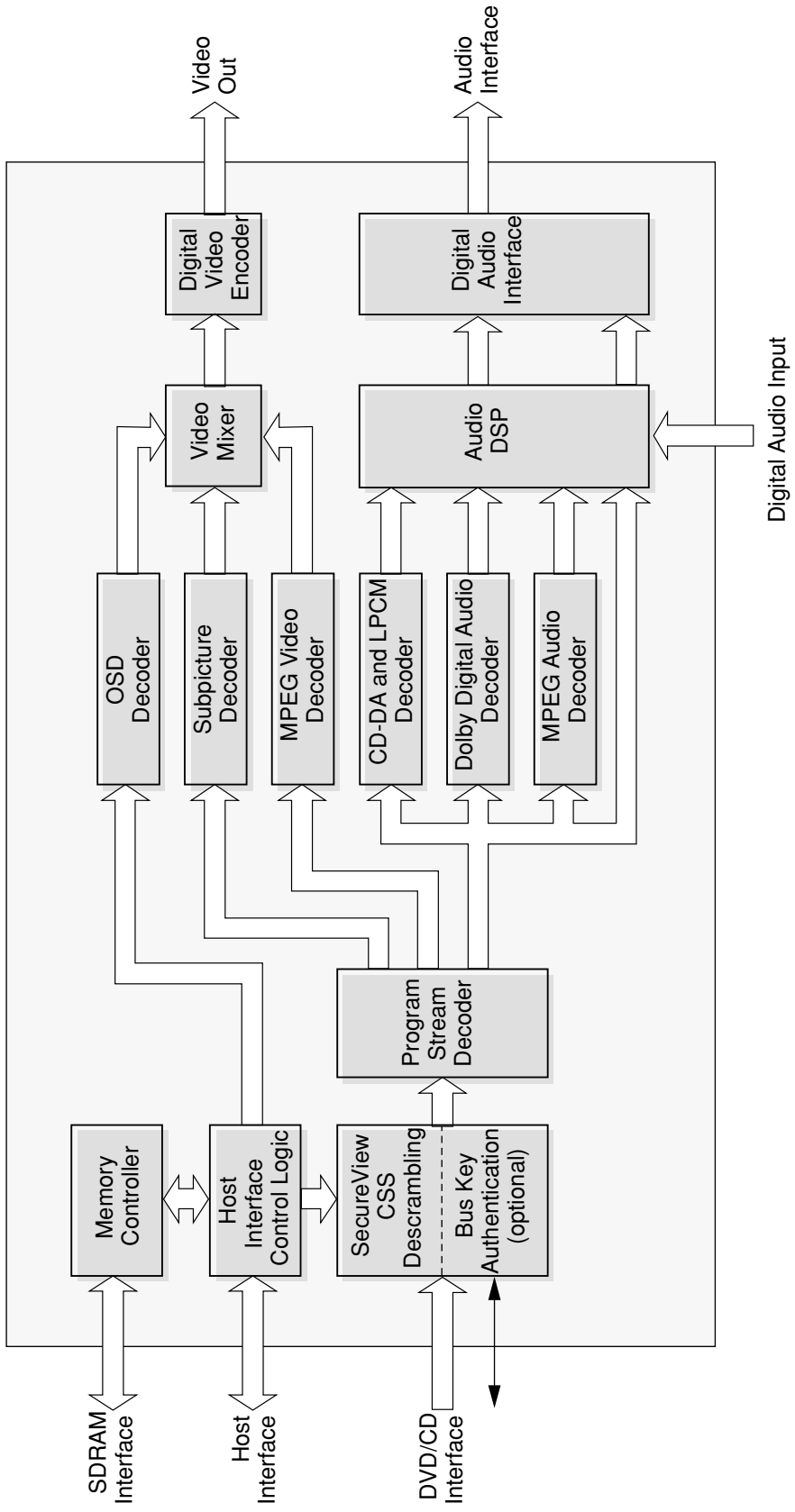
No	Name	I/O	Description
41	PVDD	P	PLL logic block VDD power supply pin
42	PLCK	O	PLCK
43	PLLLOCK	O	Frequency lock detect output (H: lock, L: unlock)
44	EFMRTD	O	Latched EFM output signal
45	PVSS	P	PLL logic block VSS power supply pin
46	RVCO	I	Resistor pin for VCO gain
47	RFD	I	Gain adjust resister for frequency detector
48	RPD	I	Gain adjust resister for phase detector
49	VCTL	I	control voltage for VCO
50	MAGIC0	I	Input for controlling hysteresis of the FD output (for testing)
51	EFMOA	I	EFM offset adjustment pin
52	TZCO	O	Tracking zero cross output pin
53	SVDD	P	Servo CPU VDD power supply pin
54	EQCTL	O	EQ control signal
55	EFMI	I	EFM signal for test
56	EFMO	O	EFM signal
57	LPFDVD	I	Asymmetric input signal for DVD
58	LPFCD	I	Asymmetric input signal for CD
59	RFI	I	Rf input signal
60	SVSS	P	Servo CPU VSS power supply pin
61	AVSS	P	Analog block VSS power supply pin
62	SME	I	Spindle error input pin
63	VREF	I	Reference voltage input pin
64	TE	I	Tracking error signal input pin
65	FE	I	Focus error signal input pin
66	ENV	I	RF envelope input pin
67	TILTI	I	TILT in (reserved)
68	AVDD	P	Analog block VDD power supply pin
69	TILTO	O	TILT out (reserved)
70	DVCTL	O	Depth variation control signal output pin
71	TBAL	O	Tracking balance signal output pin
72	FBAL	O	Focus balance signal output pin
73	SLD	O	Sled motor drive signal output pin
74	SPD	O	Spindle motor drive signal output pin
75	FOD	O	Focus actuator drive signal output pin
76	TRD	O	Tracking actuator drive signal output pin
77	TZCA	I	TE signal for tracking zero cross input pin
78	MDOUT0	O	Mode data0 out controlled by micom
79	MDOUT1	O	Mode data1 out controlled by micom
80	MDOUT2	O	Mode data2 out controlled by micom

2-1-10 SIC4 (KA3017 ; Motor & Actuator Driver)



No.	Symbol	I/O	Description
1	VH	I	HALL BIAS
2	FG	O	FG SIGNAL OUTPUT
3	ECR	I	TORQUE CONTROL REFERENCE
4	EC	I	TORQUE CONTROL SIGNAL
5	VCC2	—	SUPPLY VOLTAGE
6	PC1	—	PHASE COMPENSATION CAPACITOR
7	SIGGND	—	SIGNAL GROUND
8	VM	—	MOTOR SUPPLY VOLTAGE
9	CS1	I	CURRENT SENSOR
10	S/S	I	START/STOP
11	DIR	O	3-PHASE ROTATIONAL DIRECTION OUTPUT
12	SB	I	SHORT BRAKE
13	PWRGND	—	POWER GROUND
14	A3	O	3-PHASE OUTPUT 3
15	A2	O	3-PHASE OUTPUT 2
16	A1	O	3-PHASE OUTPUT 1
17	OPIN+	I	OP AMP INPUT (+)
18	OPIN-	I	OP AMP INPUT (-)
19	OPOUT	O	OP AMP OUTPUT
20	VCC1	—	SUPPLY VOLTAGE
21	AVM12	—	BTL CH-1, 2 MOTOR SUPPLY VOLTAGE
22	DI4	I	BTL DRIVE INPUT 4
23	DI3	I	BTL DRIVE INPUT 3
24	DI2	I	BTL DRIVE INPUT 2
25	DI1	I	BTL DRIVE INPUT 1
26	DO1-	O	BTL DRIVE 1 OUTPUT (-)
27	DO1+	O	BTL DRIVE 1 OUTPUT (+)
28	DO2-	O	BTL DRIVE 2 OUTPUT (-)
29	DO2+	O	BTL DRIVE 2 OUTPUT (+)
30	BTLPGND1	—	BTL POWER GROUND 1
31	BTLPGND2	—	BTL POWER GROUND 2
32	DO3-	O	BTL DRIVE 3 OUTPUT (-)
33	DO3+	O	BTL DRIVE 3 OUTPUT (+)
34	AVM3	—	BTL CH3 MOTOR SUPPLY VOLTAGE
35	DO4-	O	BTL DRIVE 4 OUTPUT (-)
36	DO4+	O	BTL DRIVE 4 OUTPUT (+)
37	MUTE4	I	BTL DRIVE MUTE CH 4
38	MUTE3	I	BTL DRIVE MUTE CH 3
39	MUTE12	I	BTL DRIVE MUTE CH 1, 2
40	AVM4	—	BTL CH 4 MOTOR SUPPLY VOLTAGE
41	BIAS	—	BTL BIAS VOLTAGE
42	BTLSGND	—	BTL DRIVE SIGNAL GROUND
43	H1-	I	HALL1(-) INPUT
44	H1+	I	HALL1(+) INPUT
45	H2-	I	HALL2(-) INPUT
46	H2+	I	HALL2(+) INPUT
47	H3-	I	HALL3(-) INPUT
48	H3+	I	HALL3(+) INPUT

2-1-11 ZIC1 (ZIVA 4.1 ; A/V Decoder)



Pin No.	Pin Name	I/O Voltage	I/O Type
1	$\overline{RD}$	3.3V	I
2	R/$\overline{W}$	3.3V	I
3	VDD_3.3	3.3V	
4	$\overline{WAIT}$	3.3V	O, OD, PU
5	$\overline{RESET}$	3.3V	I
6	VSS	GROUND	
7	VDD_3.3	3.3V	
8	$\overline{INT}$	3.3V	O, OD, PU
9	NC	No Connect	O
10	NC	No Connect	O
11	NC	No Connect	O
12	NC	No Connect	O
13	VDD_2.5	2.5V	
14	VSS	GROUND	
15	NC	No Connect	O
16	NC	No Connect	O
17	NC	No Connect	O
18	NC	No Connect	O
19	VSS	GROUND	
20	VDD_3.3	3.3V	
21	VDATA0	3.3V	O
22	VDATA1	3.3V	O
23	VDATA2	3.3V	O
24	VDATA3	3.3V	O
25	VDATA4	3.3V	O
26	VDATA5	3.3V	O
27	VDATA6	3.3V	O
28	VDATA7	3.3V	O
29	$\overline{VSYNC}$	3.3V	I/O
30	$\overline{HSYNC}$	3.3V	I/O
31	VSS	GROUND	
32	VDD_3.3	3.3V	
33	RESERVED	3.3V	I
34	RESERVED	3.3V	I
35	RESERVED	3.3V	I
36	VDD_2.5	2.5V	
37	VSS	GROUND	
38	RESERVED	3.3V	I
39	RESERVED	3.3V	I
40	RESERVED	3.3V	I
41	RESERVED	3.3V	I
42	RESERVED	3.3V	I
43	PIO0	3.3V	I/O
44	VSS	GROUND	
45	VDD_3.3	3.3V	
46	PIO1	3.3V	I/O
47	PIO2	3.3V	I/O
48	PIO3	3.3V	I/O

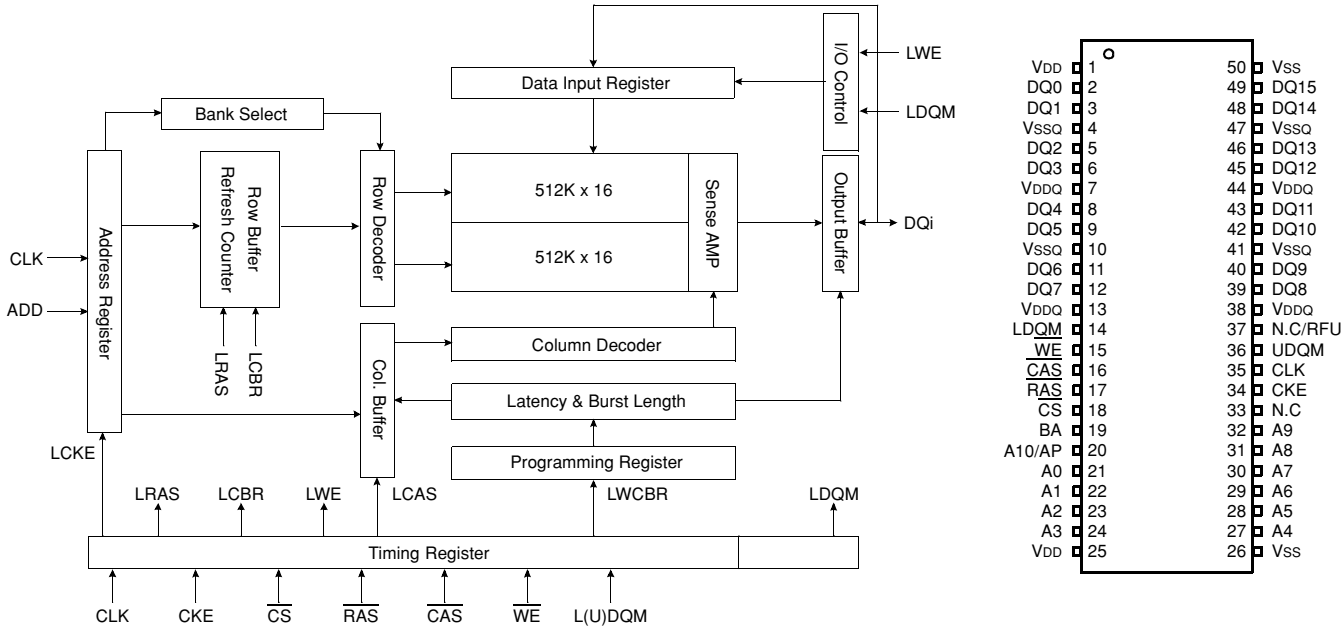
Pin No.	Pin Name	I/O Voltage	I/O Type
49	PIO4	3.3V	I/O
50	PIO5	3.3V	I/O
51	PIO6	3.3V	I/O
52	PIO7	3.3V	I/O
53	MDATA0	3.3V	I/O
54	MDATA1	3.3V	I/O
55	VDD_3.3	3.3V	
56	VSS	GROUND	
57	MDATA2	3.3V	I/O
58	MDATA3	3.3V	I/O
59	MDATA4	3.3V	I/O
60	MDATA5	3.3V	I/O
61	MDATA6	3.3V	I/O
62	MDATA7	3.3V	I/O
63	MDATA15	3.3V	I/O
64	VDD_3.3	3.3V	I/O
65	VSS	GROUND	I/O
66	MDATA14	3.3V	I/O
67	VDD_2.5	2.5V	
68	VSS	GROUND	
69	MDATA13	3.3V	I/O
70	MDATA12	3.3V	I/O
71	MDATA11	3.3V	I/O
72	MDATA10	3.3V	I/O
73	MDATA9	3.3V	I/O
74	VDD_3.3	3.3V	
75	VSS	GROUND	
76	MDATA8	3.3V	I/O
77	LDQM	3.3V	O
78	SD-CLK	3.3V	O
79	CLKSEL	3.3V	I
80	MADDR9	3.3V	O
81	MADDR8	3.3V	O
82	VDD_3.3	3.3V	
83	VSS	GROUND	
84	MADDR7	3.3V	O
85	MADDR6	3.3V	O
86	MADDR5	3.3V	O
87	VDD_2.5	2.5V	
88	VSS	GROUND	
89	MADDR4	3.3V	O
90	$\overline{MWE}$	3.3V	O
91	$\overline{SD\text{-}CAS}$	3.3V	O
92	VDD_3.3	3.3V	
93	VSS	GROUND	
94	$\overline{SD\text{-}RAS}$	3.3V	O
95	$\overline{SD\text{-}CS0}$	3.3V	O
96	$\overline{SD\text{-}CS1}$/MADDR11	3.3V	O

Pin No.	Pin Name	I/O Voltage	I/O Type
97	$\overline{SD\text{-}BS}$	3.3V	O
98	MADDR10	3.3V	O
99	MADDR0	3.3V	O
100	VDD_3.3	3.3V	
101	VSS	GROUND	
102	MADDR1	3.3V	O
103	MADDR2	3.3V	O
104	MADDR3	3.3V	O
105	RESERVED	ANALOG GND	
106	NC	No connect	O
107	NC	No connect	O
108	RESERVED	3.3V	I
109	NC	No connect	O
110	RESERVED	3.3V	I
111	RESERVED	3.3V ANALOG	
112	RESERVED	3.3V	I
113	DAI-LRCK	3.3V	I/O
114	DAI-BCK	3.3V	I/O
115	VDD_3.3	3.3V	
116	VSS	GROUND	
117	DAI-DATA	3.3V	I/O
118	DA-DATA3	3.3V	O
119	DA-DATA2	3.3V	O
120	DA-DATA1	3.3V	O
121	DA-DATA0	3.3V	O
122	DA-LRCK	3.3V	O
123	VDD_3.3	3.3V	
124	VSS	GROUND	
125	DA-XCK	3.3V	I/O
126	DA-BCK	3.3V	O
127	DA-IEC	3.3V	O
128	VDD_2.5	2.5V	
129	VSS	GROUND	
130	NC	No Connect	O
131	VSS_DAC	ANALOG GND	
132	VSS_VIDEO	ANALOG GND	
133	CVBS + sync	3.3V ANALOG	O
134	VDD_DAC	3.3V ANALOG	O
135	VDD_VIDEO	3.3V ANALOG	
136	NC	No Connect	O
137	VSS_DAC	ANALOG GND	
138	VSS_VIDEO	ANALOG GND	
139	CVBS/G/Y	3.3V ANALOG	O
140	VDD_DAC	3.3V ANALOG	
141	VDD_VIDEO	3.3V ANALOG	
142	NC	No Connect	O
143	VSS_DAC	ANALOG GND	

Pin No.	Pin Name	I/O Voltage	I/O Type
144	VSS_VIDEO	ANALOG GND	
145	Y/B/U	3.3V ANALOG	O
146	VDD_DAC	3.3V ANALOG	
147	VDD_VIDEO	3.3V ANALOG	
148	NC	No Connect	O
149	VSS_DAC	ANALOG GND	
150	VSS_VIDEO	ANALOG GND	
151	C/R/V	3.3V ANALOG	O
152	VDD_DAC	3.3V ANALOG	
153	VDD_VIDEO	3.3V ANALOG	
154	VSS_RREF	ANALOG GND	
155	RREF	3.3V ANALOG	O
156	VDD_RREF	3.3V ANALOG	
157	A_VSS	GROUND	
158	SYSCLK	3.3V	I
159	VCLK	3.3V	I
160	A_VDD	3.3V ANALOG	
161	DVD-DATA0/CD-DATA	3.3V	I
162	DVD-DATA1/CD-LRCK	3.3V	I
163	DVD-DATA2/CD-BCK	3.3V	I
164	DVD-DATA3/CD-C2P0	3.3V	I
165	DVD-DATA4/CDG-SDATA	3.3V	I
166	VSS	GROUND	
167	VDD_3.3	3.3V	
168	DVD-DATA5/CDG-VFSY	3.3V	I
169	DVD-DATA6/CDG-S0S1	3.3V	I
170	DVD-DATA7/CDG-SCLK	3.3V	I
171	VDACK	3.3V	I
172	VREQUEST	3.3V	O
173	VSTROBE	3.3V	I
174	ERROR	3.3V	I
175	VDD_3.3	3.3V	
176	RESERVED	GROUND	
177	VDD_3.3	3.3V	
178	VSS	GROUND	
179	NC	No connect	O
180	NC	No connect	O
181	NC	No connect	O
182	HADDR0	3.3V	I
183	HADDR1	3.3V	I
184	HADDR2	3.3V	I
185	RESERVED	3.3V	I
186	RESERVED	3.3V	I
187	RESERVED	3.3V	I
188	VSS	GROUND	
189	VDD_2.5	2.5V	
190	RESERVED	3.3V	I

Pin No.	Pin Name	I/O Voltage	I/O Type
191	VSS	GROUND	
192	VDD_3.3	3.3V	
193	RESERVED	3.3V	I
194	RESERVED	3.3V	I
195	RESERVED	3.3V	I
196	RESERVED	3.3V	I
197	HDATA7	3.3V	I/O
198	VSS	GROUND	
199	HDATA6	3.3V	I/O
200	HDATA5	3.3V	I/O
201	HDATA4	3.3V	I/O
202	HDATA3	3.3V	I/O
203	HDATA2	3.3V	I/O
204	VDD_3.3	3.3V	
205	VSS	3.3V	
206	HDATA1	3.3V	I/O
207	HDATA0	3.3V	I/O
208	$\overline{CS}$	3.3V	I

2-1-12 ZIC2/ZIC3 (KM416S1120D ; CMOS 16M SDRAM)



Pin	Name	InputFunction
CLK	System Clock	Active on the positive going edge to sample all inputs.
$\overline{CS}$	Chip Select	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and L(U)DQM
CKE	Clock Enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
A_0 ~ A_{10}/AP	Address	Row / column addresses are multiplexed on the same pins. Row address : RA_0 ~ RA_{10}, column address : CA_0 ~ CA_7
BA	Bank Select Address	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	Row Address Strobe	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	Column Address Strobe	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	Write Enable	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
L(U)DQM	Data Input/Output Mask	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when L(U)DQM active.
$DQ_{0 \sim 15}$	Data Input/Output	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	Power Supply/Ground	Power and ground for the input buffers and the core logic.
V_{DDQ}/V_{SSQ}	Data Output Power/Ground	Isolated power supply and ground for the output buffers to provide improved noise immunity.
N.C/RFU	No Connection/ Reserved for Future Use	This pin is recommended to be left No Connection on the device.

MEMO

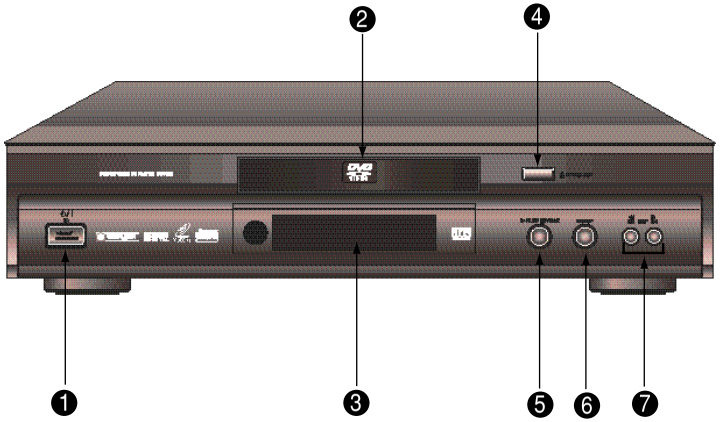
3. Product Specifications

GENERAL	Power Requirements	AC 120V, 60Hz
	Power Consumption	17W
	Weight	3.1kg
	Dimensions	W 430mm X D 280mm X 89mm
	Operating Temperature Range	+5˚C ~ +35˚C
	Operating Humidity Range	10% to 75%
DISC	DVD (Digital Versatile Disc)	Reading Speed : 3.49 m/sec
		Approx. Play Time (Single Sided, Single Layer Disc) : 135 min.
	CD : 12Cm (Compact Disc)	Reading Speed : 1.2 to 1.4 m/sec
		Maximum Play Time : 74min.
	CD : 8Cm (Compact Disc)	Reading Speed : 1.2to 1.4 m/sec.
		Maximum Play Time : 20min.
	VCD : 12Cm	Reading Speed : 1.2 to 1.4 m/sec.
		Maximum Play Time : 74min. (Video + Audio)
Video Output	Composite Video	1 channel : 1.0Vp-p (75ohm load)
	Component Video	Y : 1.0Vp-p (75ohm load) ; DV-P305U Only
		Pr : 0.70Vp-p (75ohm load) ; DV-P305U Only
		Pb : 0.70Vp-p (75ohm load) ; DV-P305U Only
	S-Video	Luminance Signal : 1Vp-p (75ohm load)
		Color Signal : 0.286Vp-p (75ohm load)
Audio Output	2 Channel	L (1/L), R (2/R)
	* Frequency Response	48kHz Sampling : 4Hz to 22kHz
		96kHz Sampling : 4Hz to 44kHz
	* S/N Ratio	115dB
	* Dynamic Range	105dB
	* Total Harmonic Distortion	0.003%

* : Nominal specification

MEMO

Description-Front Panel



Front Panel Controls

❶ **STANDBY / ON**
- When the unit is first plugged in, the indicator lights. When STANDBY/ON is pressed, the lamp goes out and the player is turned on.

❷ **DISC TRAY**
- Press OPEN/CLOSE to open and close the disc tray.

❸ **DISPLAY**
- Operation indicators are displayed here.

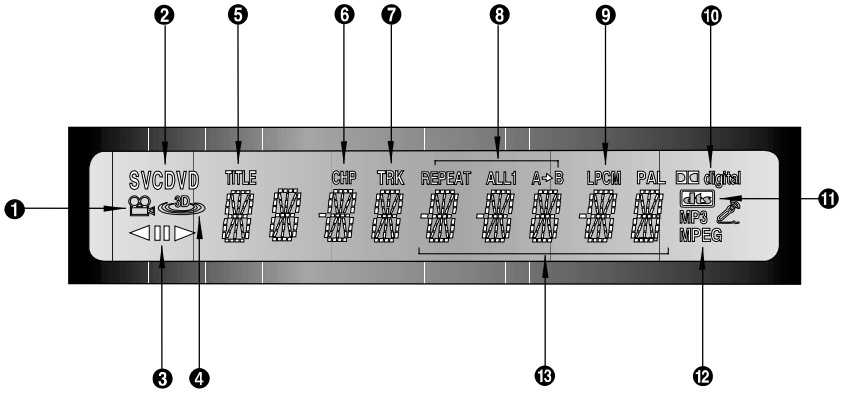
❹ **OPEN/CLOSE**
- Press to open and close the disc tray.

❺ **PLAY/PAUSE**
- Begin or pause disc play.

❻ **STOP**
- Stops disc play.

❼ **SKIP**
- Use to skip a scene or music.

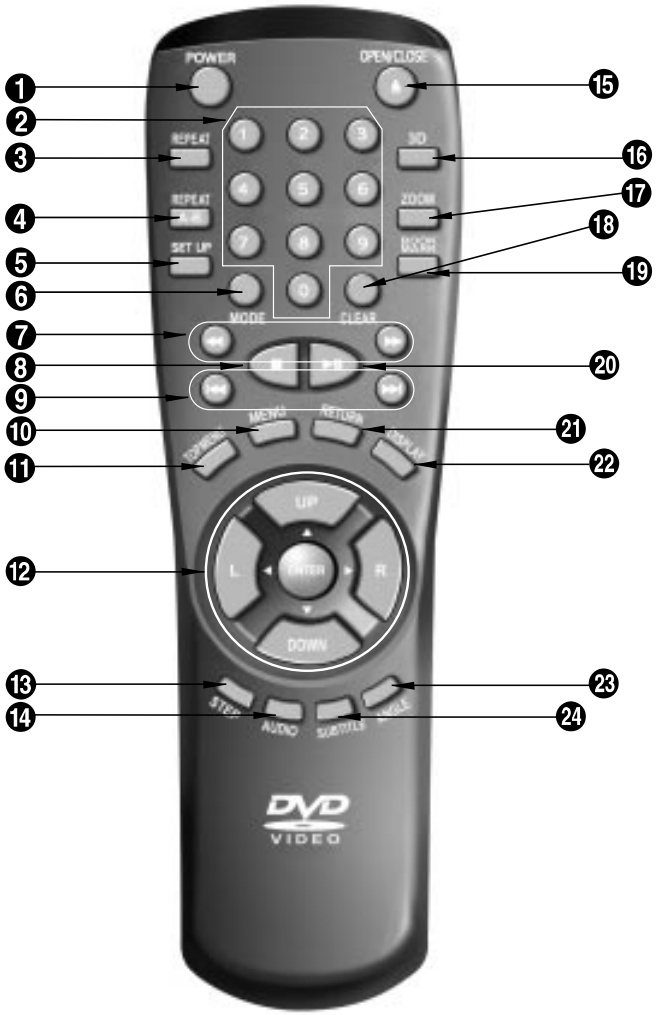
Front Panel Display



Front Panel Display

❶ You can now select different viewing points of the scene recorded by different cameras.
❷ Disc type indicators
❸ Reverse playback / Pause / Forward playback
❹ Lights when 3D surround is turned on.
❺ DVD : Title number
❻ DVD : Chapter number.
❼ Video/Audio CD : Track number
❽ Repeat play mode
❾ Linear PCM audio output
❿ Dolby Digital audio output
⓫ DTS (Digital Theater System) audio output(Digital only)
⓬ MPEG-2 Audio output
⓭ Displays various messages concerning operations such as PLAY, STOP, LOAD, RANDOM, ...
no DISC : No disc loaded.
OPEN : The disc tray is open.
LOAD : Player is loading disc information.

Tour of the Remote Control



Tour of the Remote Control

DVD Function Buttons

❶ **DVD POWER Button**
- Turns the player on and off.

❷ **NUMBER Buttons**

❸ **REPEAT Button**
- Allows you to repeat play a title, chapter, track, or disc.

❹ **A-B REPEAT Button**
- Marks a segment to repeat between A and B.

❺ **SETUP Button**
- Brings up the DVD player's Setup menu.

❻ **MODE Button**
- Allows you to program a specific order.

❼ **SEARCH Buttons**
- Allows you to search forward/backward through a disc.

❽ **STOP Button**
- To stop playback.

❾ **SKIP Buttons**
- Skip the, Chapter, or Track.

❿ **MENU Button**
- Brings up the Menu on a disc.

⓫ **TOP MENU Button**
- Brings up the Top Menu on a disc.

⓬ **ENTER/DIRECTION Button (UP/DOWN or LEFT/RIGHT Button)**

⓭ **STEP Button**
- Advances playback one frame at a time.

⓮ **AUDIO Button**
- Accesses various audio functions on a disc.

⓯ **OPEN/CLOSE Button**
- To open or close the disc tray.

⓰ **3D SOUND Button**
- To activate the 3D sound.

⓱ **ZOOM Button**
- To magnify part of picture.

⓲ **CLEAR Button**
- Removes menus or status displays from the screen.

⓳ **BOOKMARK Button**
- To rapidly return to a location of disc.

⓴ **PLAY/PAUSE Button**
- Begin/Pause disc play.

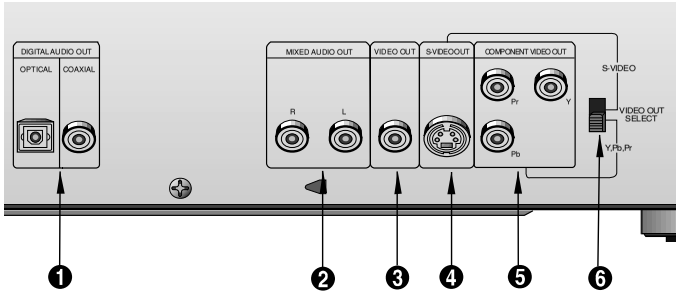
㉑ **RETURN Button**
- Returns to a previous menu.

㉒ **DISPLAY Button**
- Displays the current disc mode.

㉓ **ANGLE Button**
- Accesses various camera angles on a disc.

㉔ **SUBTITLE Button**
- Accesses various subtitles on a disc.

Description-Rear Panel



Rear Panel

❶ DIGITAL AUDIO OUT JACK
- Use either an optical or coaxial digital cable to connect to a compatible Dolby Digital receiver. Use to connect to an A/V Amplifier that contains a Dolby Digital decoder or DTS decoder.

MIXED AUDIO OUT JACKS

❷ • Connect to the Audio input jacks of your television, audio/video receiver, or VCR.

VIDEO OUT JACK

❸ • Use a video cable to connect one of the jack to the Video input on your television.

❹ • Use the S-Video cable to connect this jack to the S-Video jack on your television for a higher quality picture. The S-Video must be selected in the VIDEO OUT SELECT.

COMPONENT VIDEO OUT JACKS

❺ • Use these jacks if you have a TV with Component Video in jacks. These jacks provide Pr, Pb and Y video. Along with S-Video, Component Video provides the best picture quality. The Y, Pb, Pr must be selected in the VIDEO OUT SELECT.

VIDEO OUT SELECT SWITCH

❻ • Use the switch to set video out.
- If the Y, Pb or Pr is selected, the S-Video may not work.
- If the S-Video is selected, the Y, Pb or Pr may not work.

S-VIDEO OUT JACK

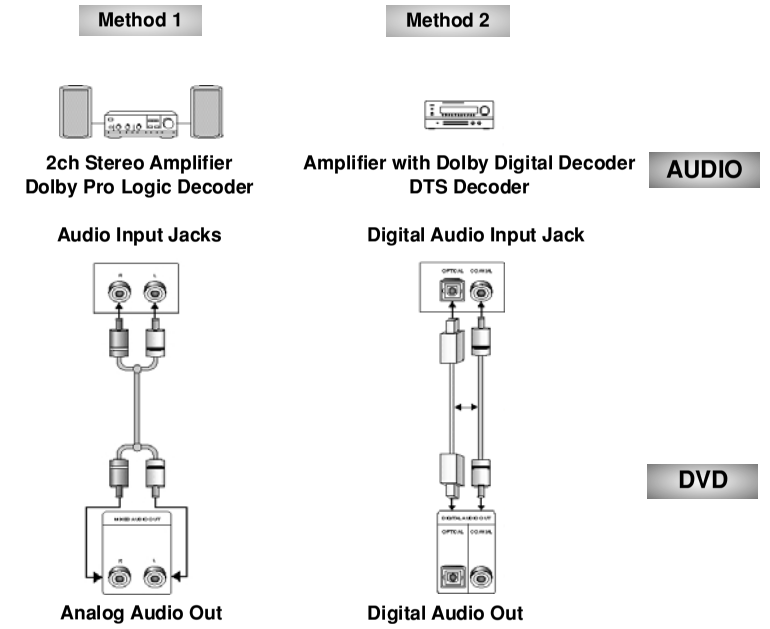
Choosing a Connection

The following show examples of connections commonly used to connect the DVD player with a TV and other components.

Before Connection the DVD Player

- Always turn off the DVD player, TV, and other components before you connect or disconnect any cables.
- Refer to owner's manual of the additional components you are connecting for more information for those particular components.

Connection to an Audio System



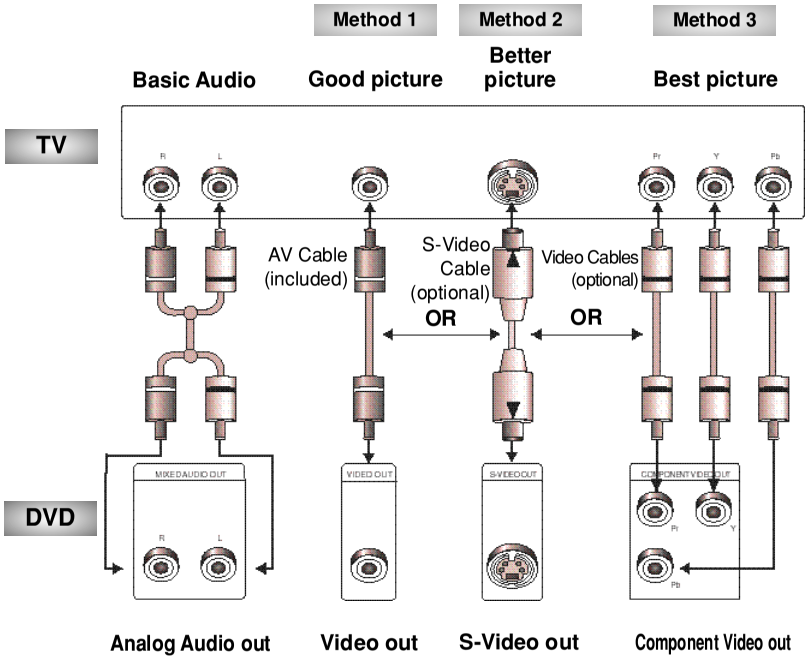
Connection to an Audio System

- **Method 1** DVD Player + 2ch Stereo Amplifier or Dolby Pro Logic Decoder
- **Method 2** DVD Player + Amplifier with Dolby Digital Decoder/DTS Decoder

Choosing a Connection

Connection to a TV

TV (Normal, Widescreen, Projection, etc..)



Connection to a TV (For Video)

- **Method 1** DVD Player + TV with Video Input Jack
- **Method 2** DVD Player + TV with S-Video Input Jack
  (If the S-Video is selected in the VIDEO OUT SELECT.)
- **Method 3** DVD Player + TV with Component Video Jacks
  (If the Y, Pb or Pr is selected in the VIDEO OUT SELECT.)

NOTE

- If the VIDEO OUT SELECT SWITCH (on the rear panel) is set to Y, Pb or Pr, the S-Video may not work.
- If the VIDEO OUT SELECT SWITCH is set to S-Video, the Y, Pb or Pr may not work.
- After correcting the switch, turn power off and then on again.

5. Disassembly and Reassembly

5-1 Cabinet and PCB

Note : Reassembly in reverse order.

5-1-1 Top Cabinet Removal

1) Remove 3 Screws ① on the back Top Cabinet.
2) Remove 2 Screws ② , ③ on the left and right side.
3) Lift up the Top Cabinet in direction of arrow.

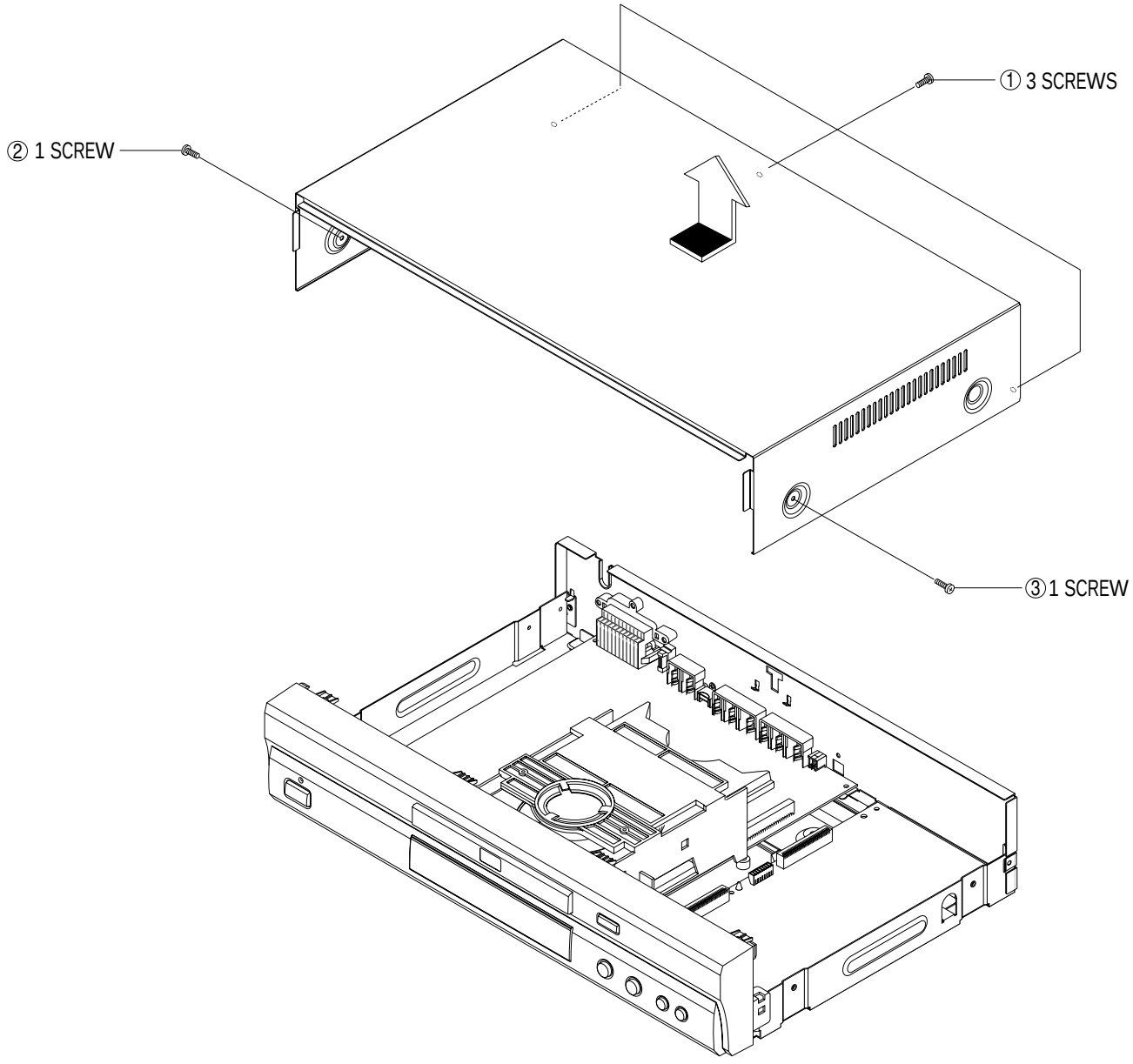


Fig. 5-1 Top Cabinet Removal

5-1-2 Door-Tray Removal

1) Supply power and open Tray ① .
2) Disassemble the Door-Tray ② in direction of arrow “A”.
3) Close Tray ① and power off.

Note : If Tray ① doesn’t open, insert a Screw driver ④ into the Emergency hole ③ (as shown in detailed drawing) and then push it in the direction of arrow “B”. Open Tray manually.

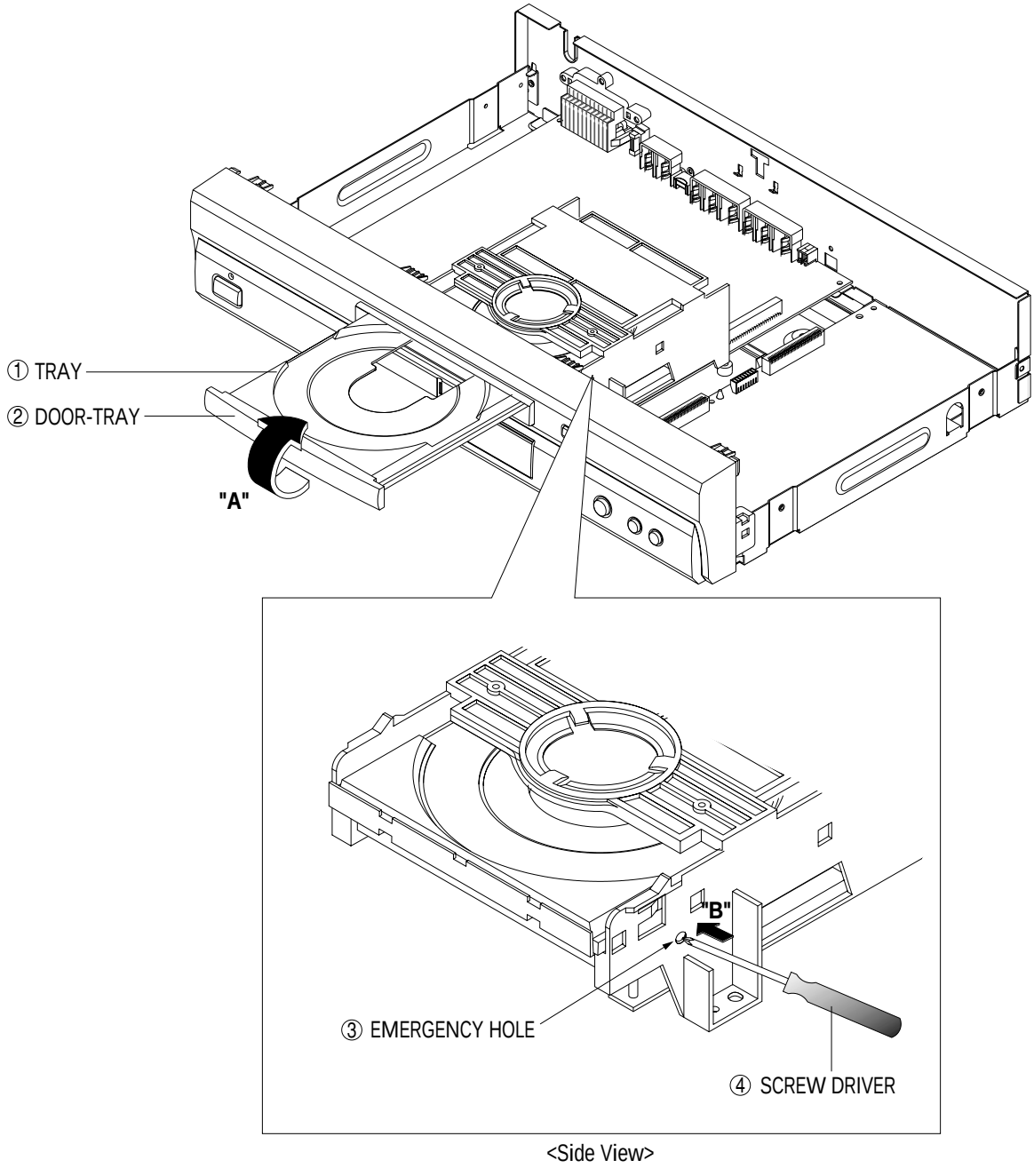


Fig. 5-2 Door-Tray Removal

5-1-3 Ass'y Front-Panel, Key PCB Removal

1) Remove Ass'y Front-Panel ①.
2) Remove 1 Screw ② and Ass'y Knob-Power ③.
3) Remove 5 Screws ④ and Key PCB ⑤.

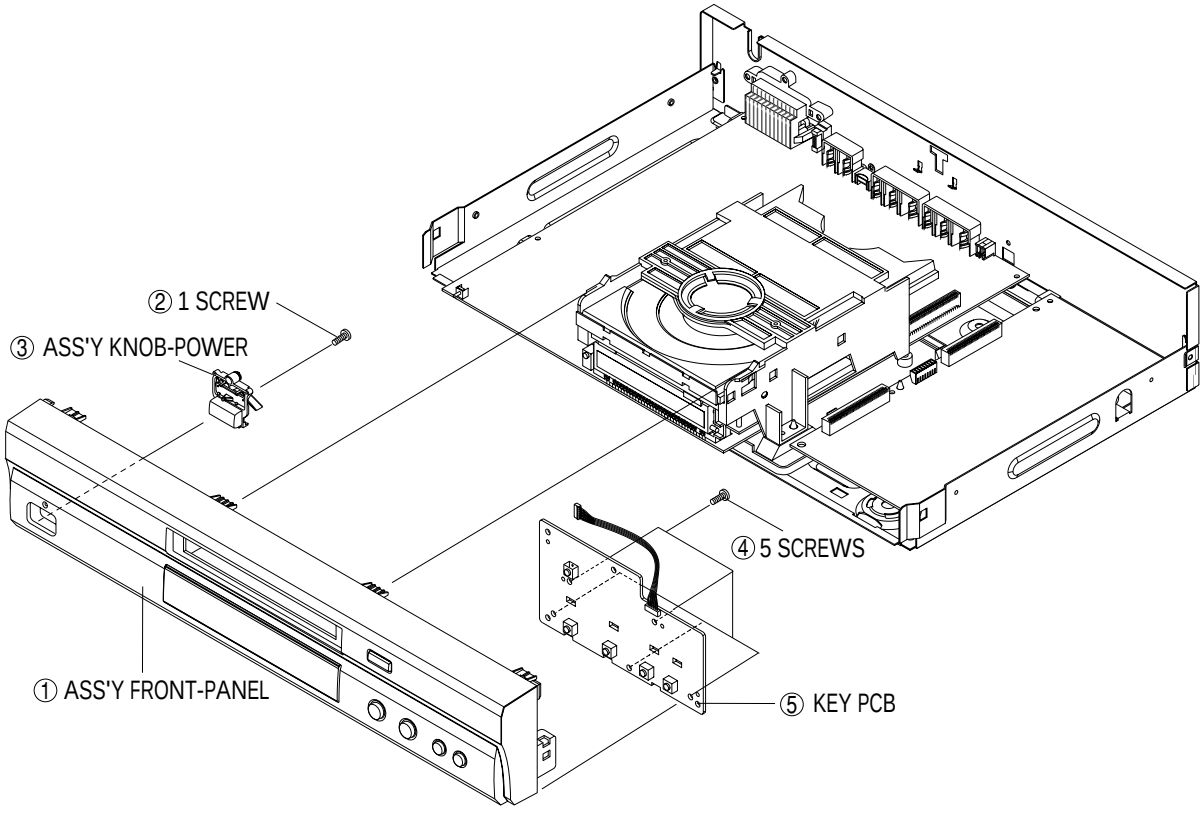


Fig. 5-3 Ass'y Front-Panel, Key PCB Removal

5-1-4 Ass'y Deck Removal

1) Remove 4 Screws ① from the Ass'y Deck and lift it up.

CAUTIONS ;
(1) When disassembling, switch the SW3 to "OFF" on the Deck PCB and remove the FPC connected to DCN1 on Main PCB.
(2) When assembling, insert the FPC into the DCN1 on Main PCB and switch SW3 to "ON" on the Deck PCB.

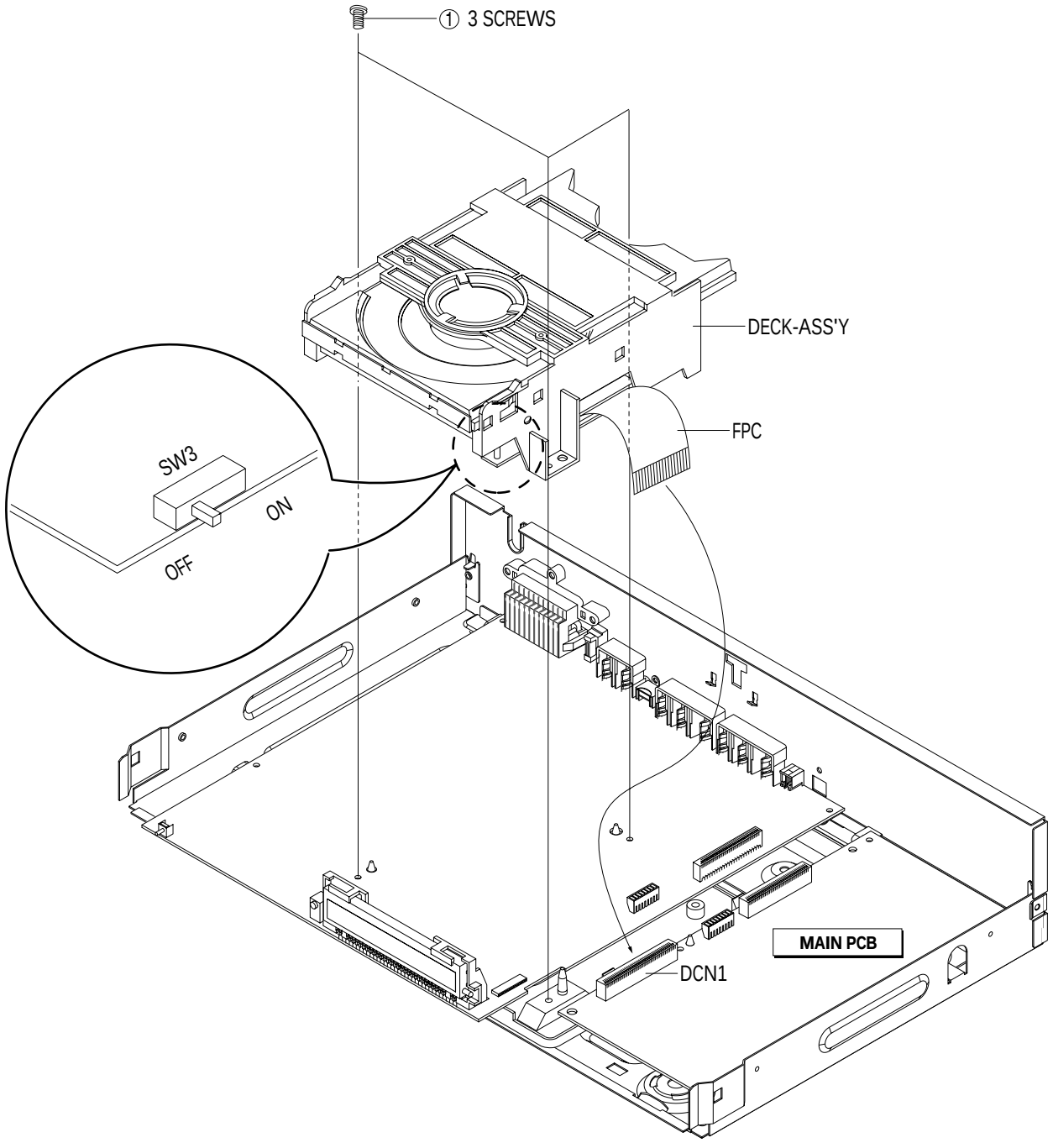


Fig. 5-4 Ass'y Deck Removal

5-1-5 Main PCB, Jack PCB Removal

1) Remove 1 Screw ①.
2) Remove 2 Screws ② and lift up the Jack PCB ③.
3) Remove 3 Screws ④ and lift up the Main PCB ⑤.

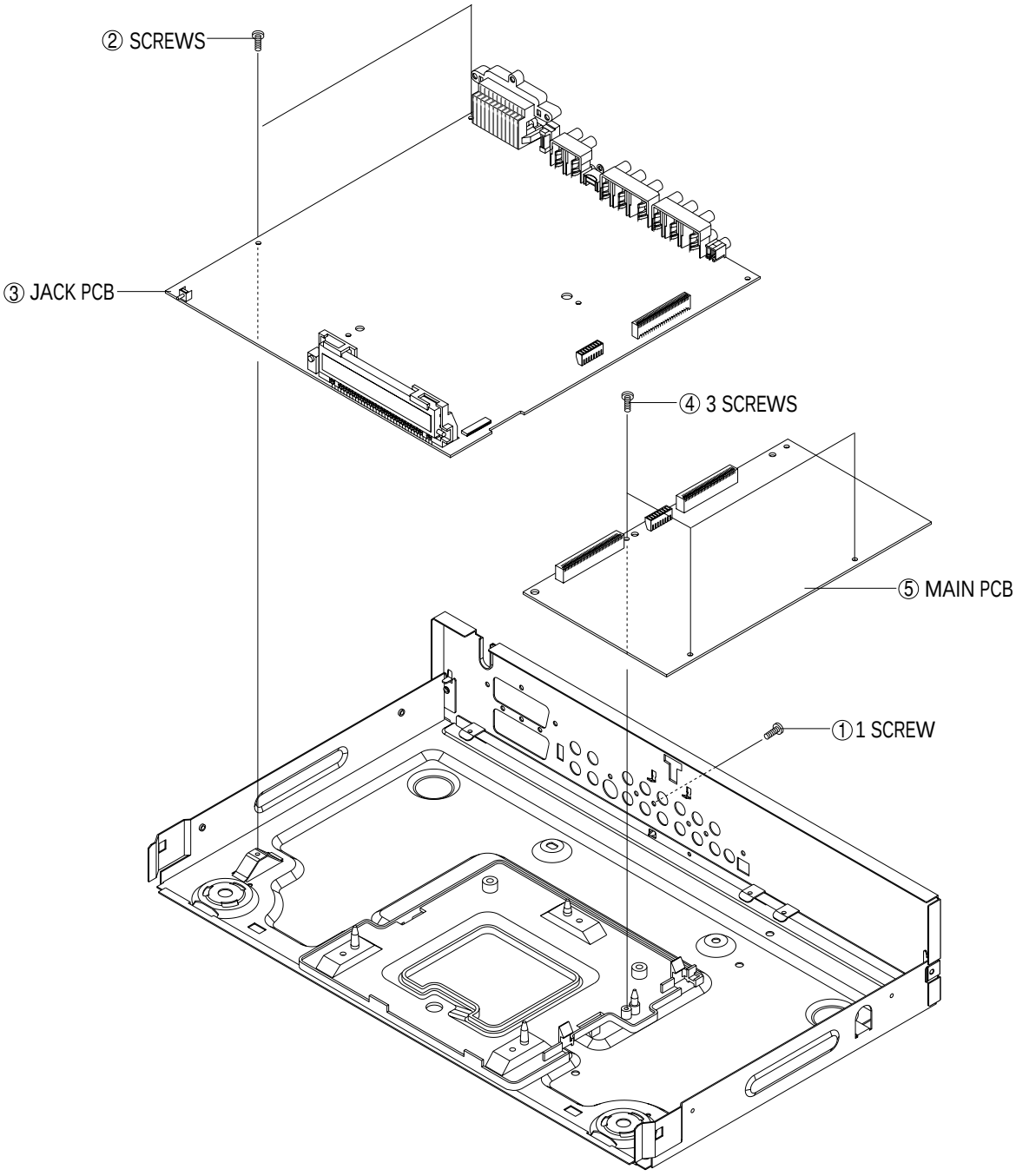


Fig. 5-5 Main PCB, Jack PCB Removal

5-2 PCB Location

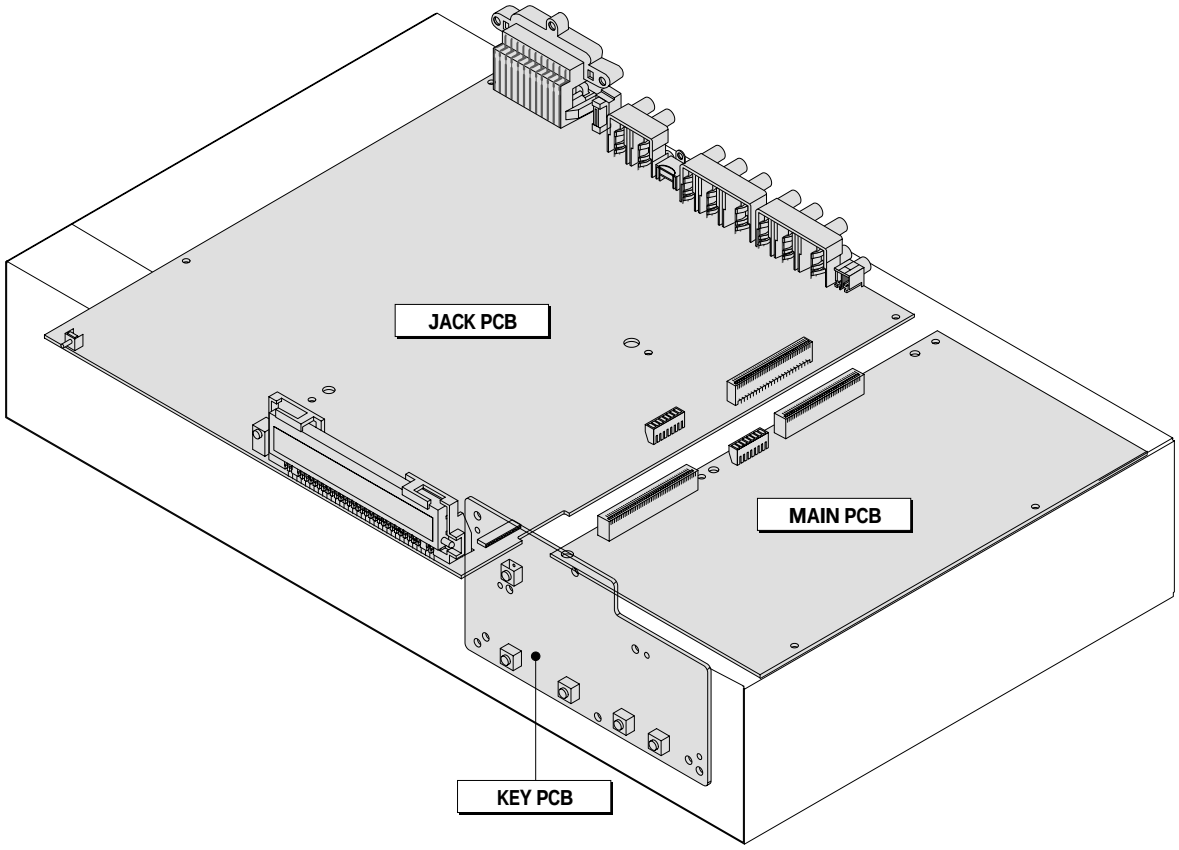
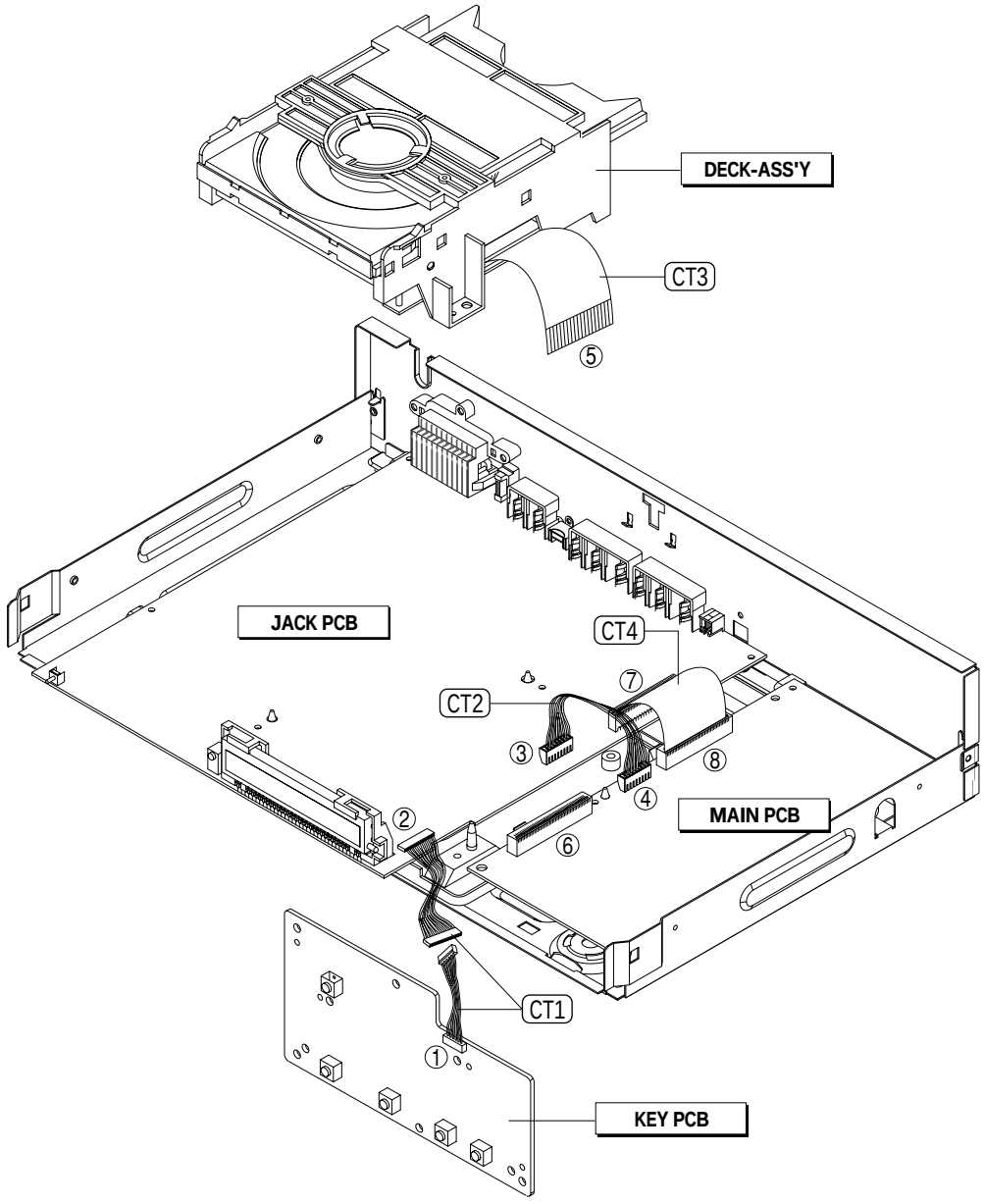


Fig. 5-6 PCB Location

5-3 Connector Diagram



NO.	CONNECTOR NO.	DIRECTION	CONNECTOR NO.	NO.
①	CON21	KEY PCB ◄—(CT1)—► JACK PCB	CN2	②
③	PCNS1	JACK PCB ◄—(CT2)—► MAIN PCB	PCN1	④
⑤	FPC	DECK-ASS'Y ◄—(CT3)—► MAIN PCB	DCN1	⑥
⑦	CN1	JACK PCB ◄—(CT4)—► MAIN PCB	CN8	⑧

Fig. 5-7 Connector Diagram

5-4 Deck

5-4-1 PCB Deck Ass'y and Ass'y P/U Deck Removal

1) Remove the soldering of SLED+, SLED- ① and TM+, TM- ②.
2) Disconnect CN3 ③, CN2 ④.
3) Remove 1 Screw ⑤ and lift up the PCB Deck ⑥.
4) Remove 1 Screw ⑦.
5) Push the Hook ⑧ in the direction of arrow "A" and lift up the Ass'y P/U Deck ⑨ in direction of arrow "B".

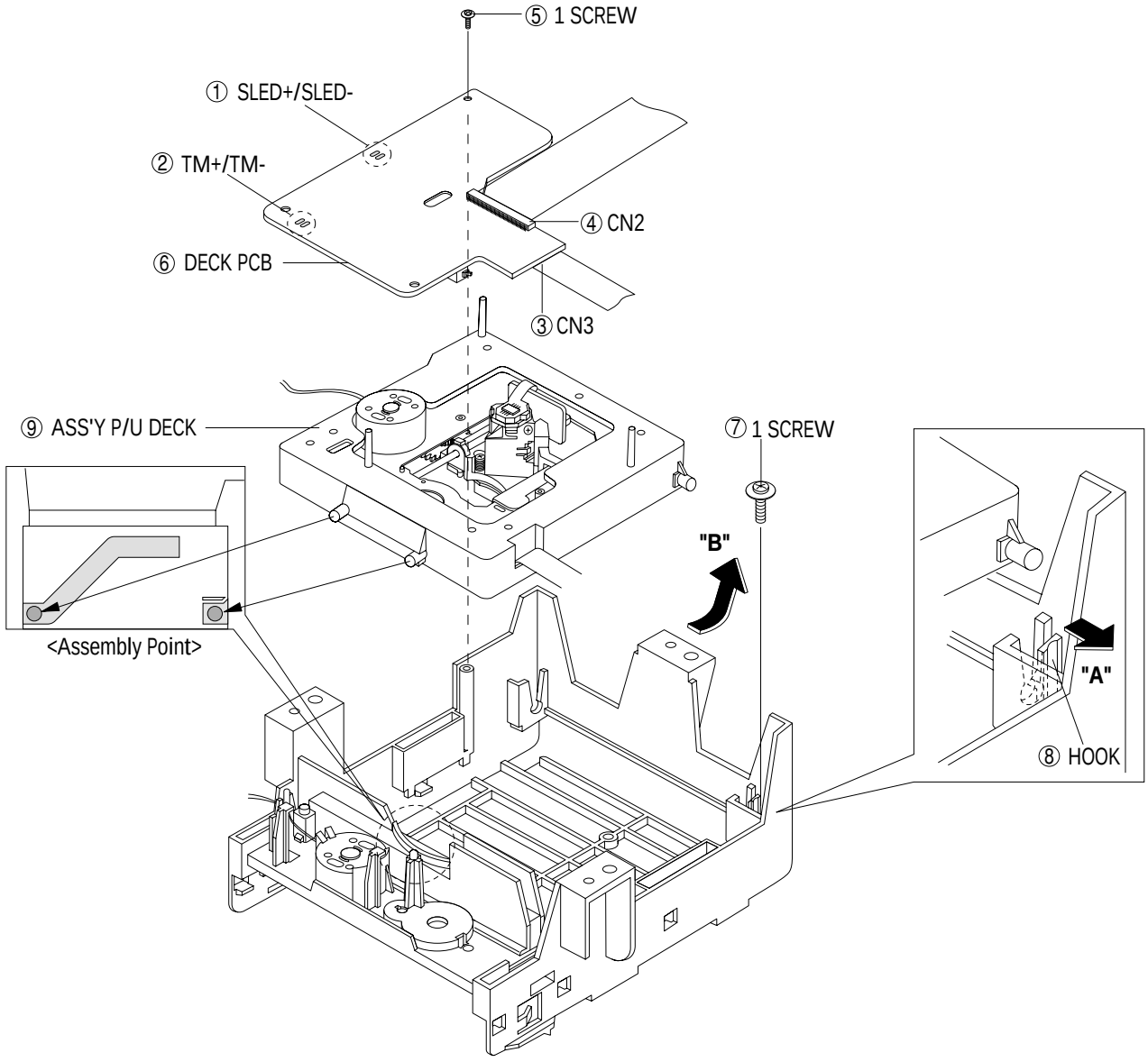


Fig. 5-8 PCB Deck Ass'y and Ass'y P/U Deck Removal

5-4-2 Tray Disc Removal

1) Insert a Screw Driver ① into Emergency Hole ② and push the Sider Housing ③ in the direction arrow “A”.
2) When the Tray Disc ④ comes out little, pull it in the direction arrow “B” by hand.
3) Pull the Tray Disc ④ to disassemble , while simultaneously pushing 2 Stoppers ⑤ (left, right) in the direction arrow “C”, “D”.

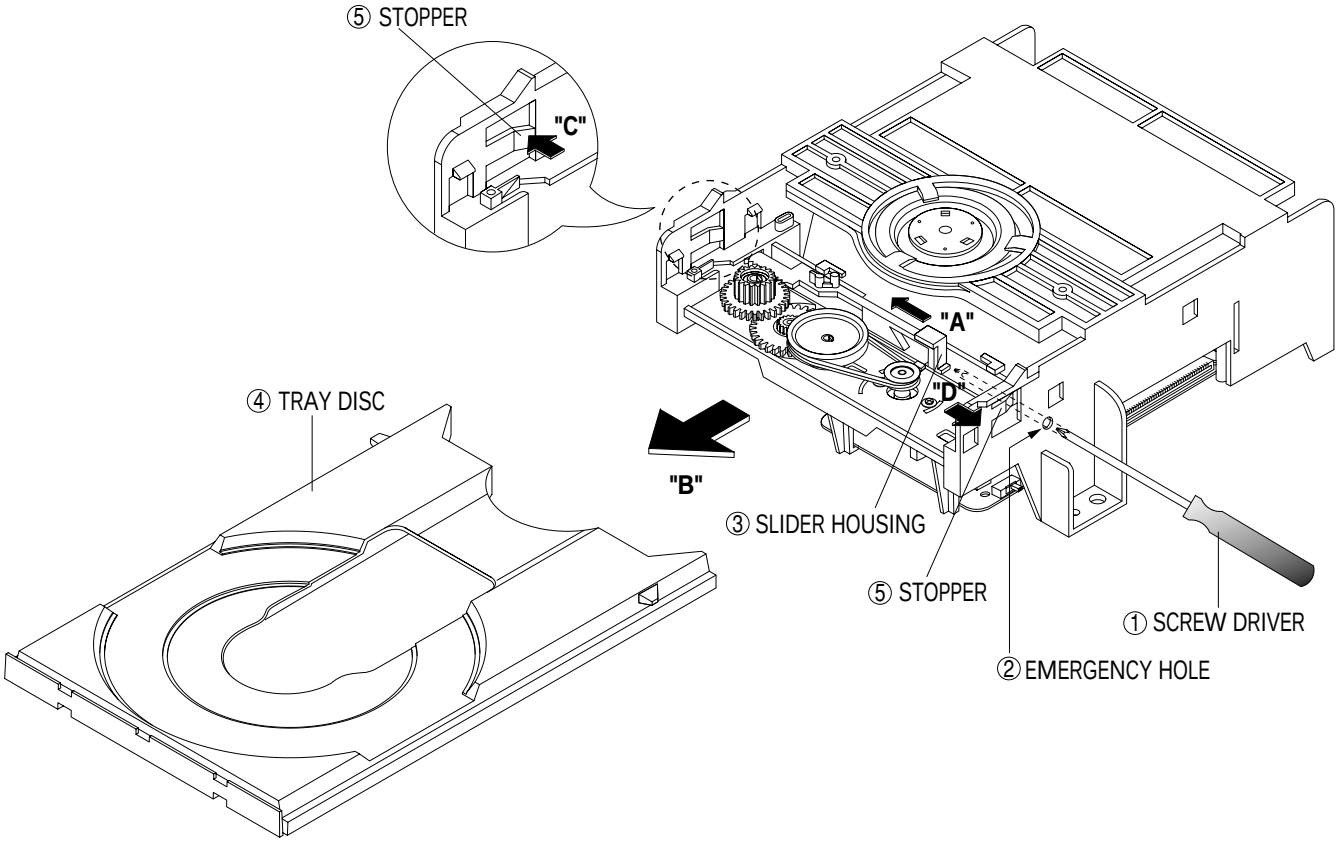


Fig. 5-9 Tray Disc Removal

5-4-3 Slider Housing Removal

1) Push the Slider Housing ① in the direction arrow “A”.
2) Lift up the Slider Housing ①.

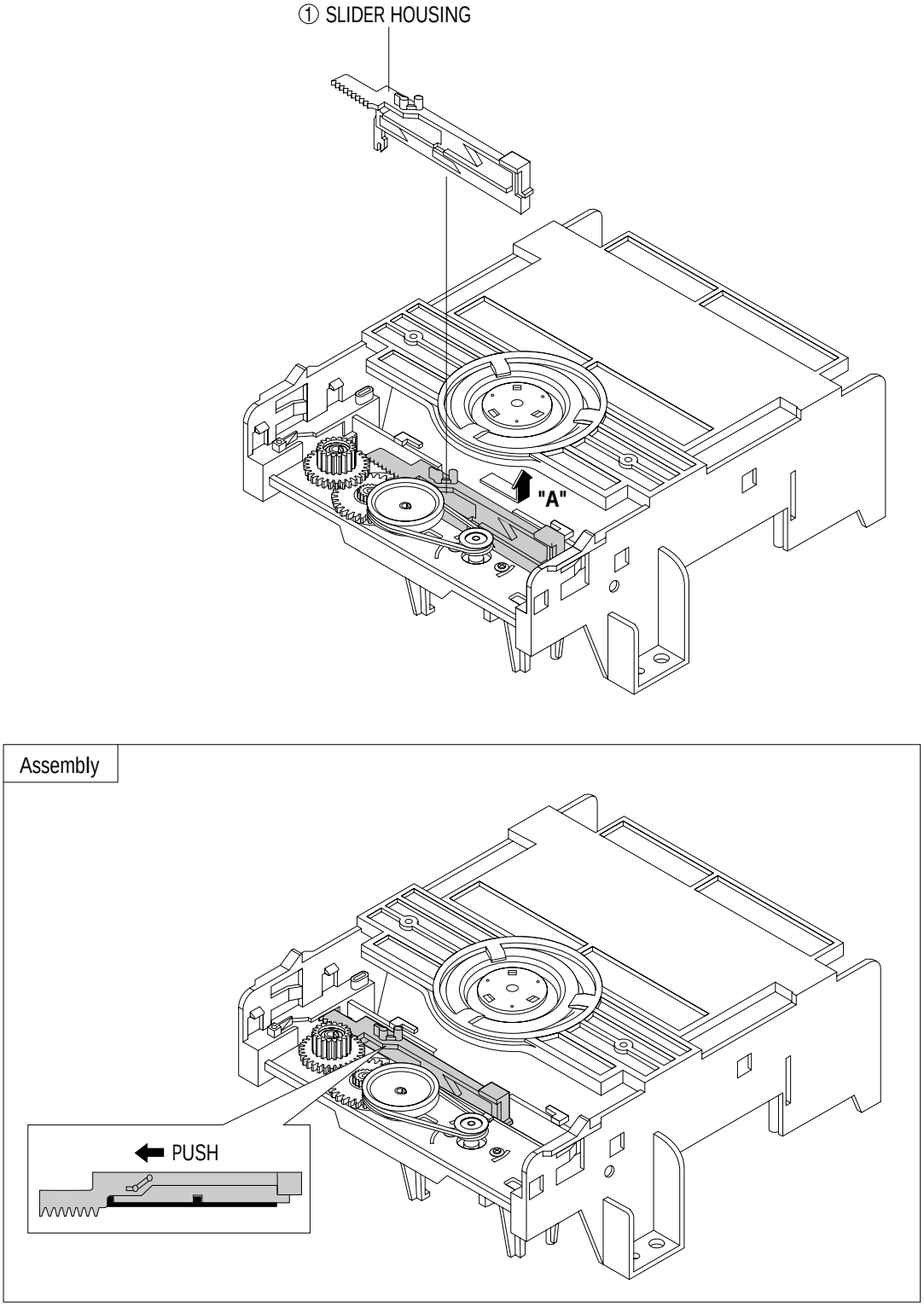


Fig. 5-10 Slider Housing Removal

5-4-4 Housing Ass'y Removal

1) Remove Belt ① and 1 Screw ②.
2) Remove 1 Screw ③ and lift up the Pulley Gear ④.
3) Push the Hook ⑤ in the direction arrow "A" and lift up Gear Tray ⑥, Gear Housing ⑦.
4) Push the 4 Hooks ⑧ bottom side in the direction arrow "B" and lift up the Motor Load Ass'y ⑨.
5) Remove Clamper Ass'y ⑩.

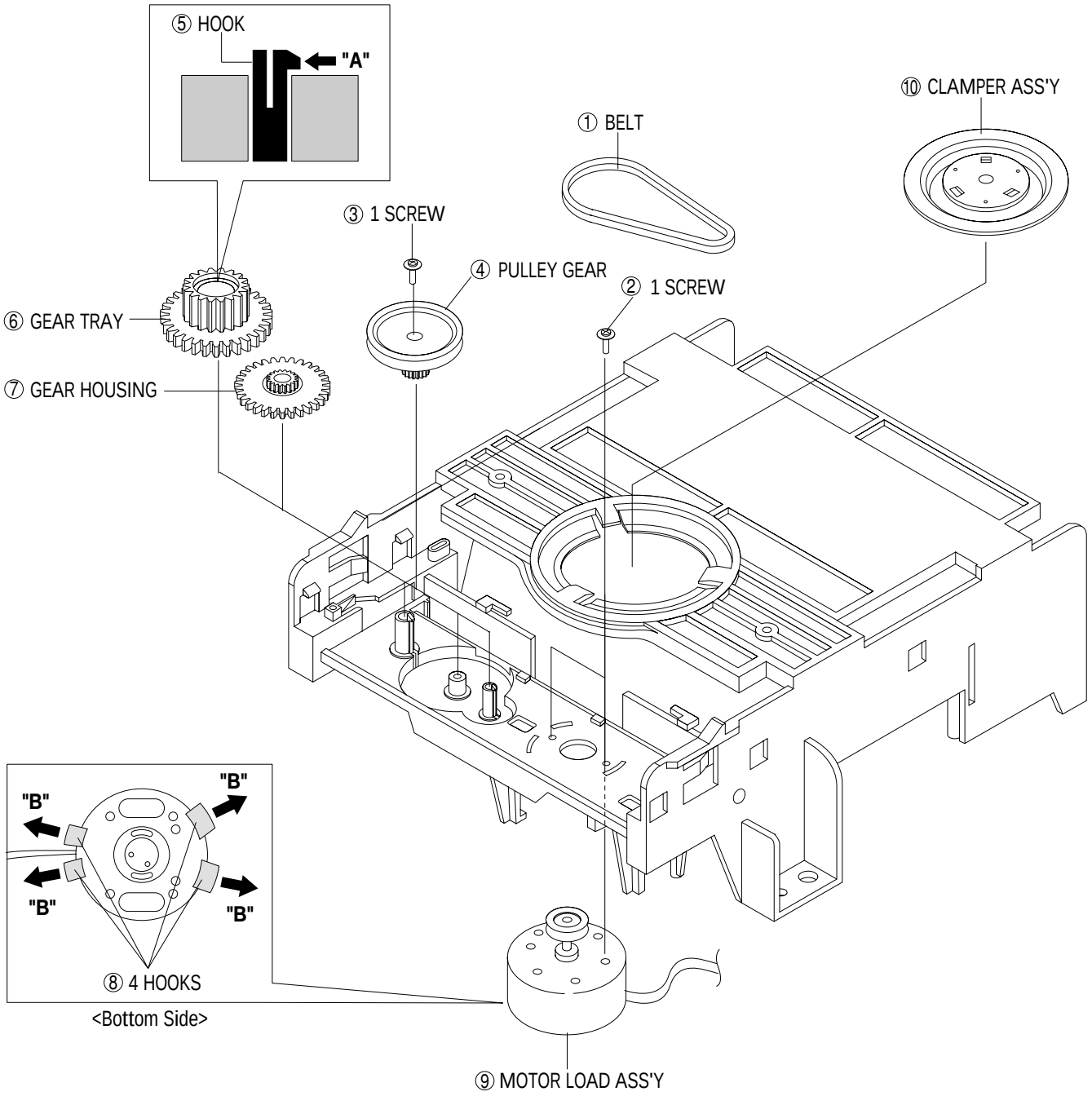


Fig. 5-11 Housing Ass'y Removal

5-4-5 Sub Chassis Removal

1) Remove the 4 Screws ①.
2) Lift up the Ass'y Brkt Deck ②.

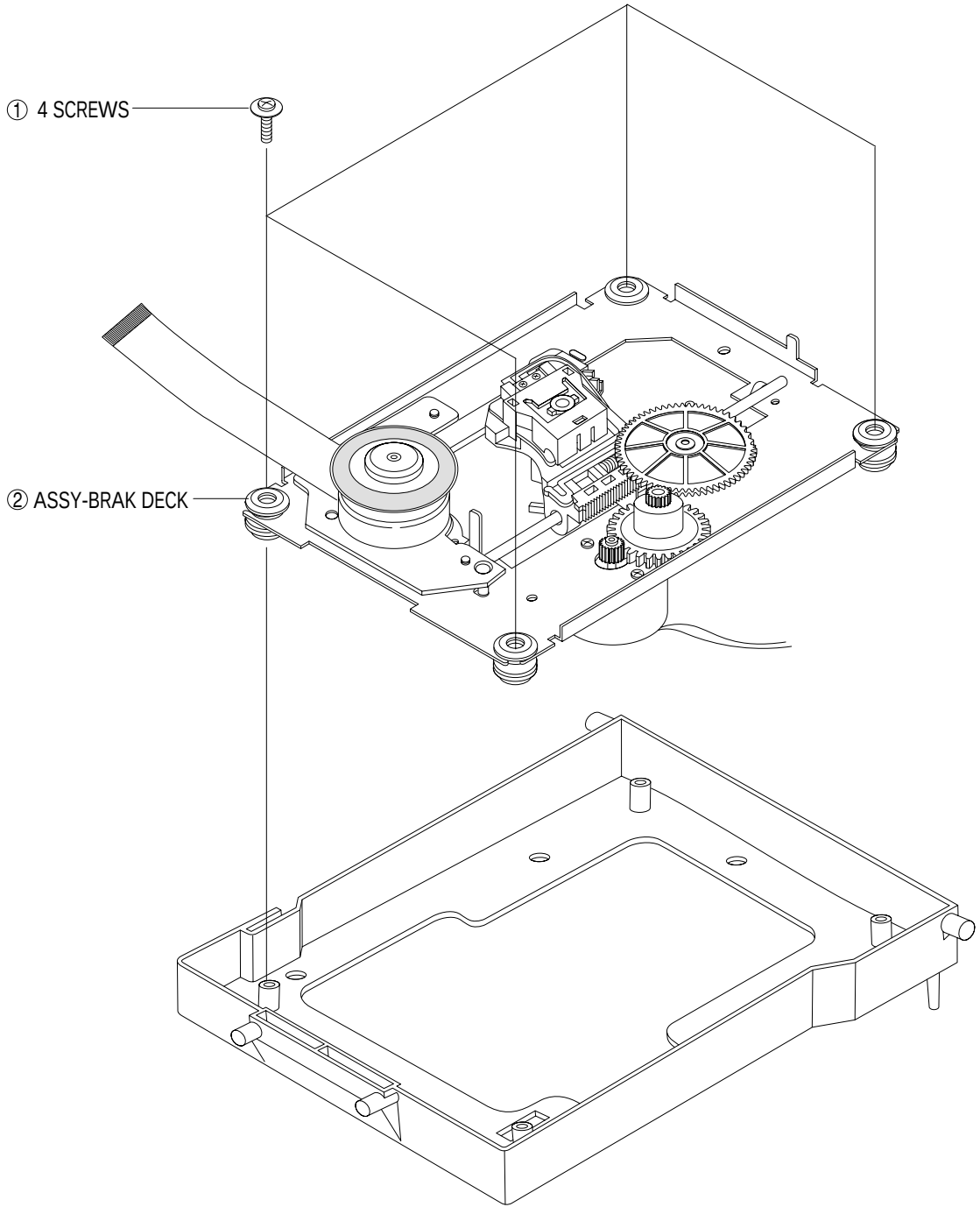


Fig. 5-12 Sub Chassis Removal

5-4-6 Ass'y Brkt Deck Removal

1) Remove Washer ①.
2) Remove Gear Feed B ② , Gear Feed A ③.
3) Remove 2 Screws ④.
4) Remove Shaft Pick-Up ⑤ and Pick-Up Assy ⑥.
5) Remove 1 Screw ⑦.
6) Remove 2 Screws ⑧.
7) Remove 3 Spring Spindle ⑨ and Motor Spindle Ass'y ⑩.

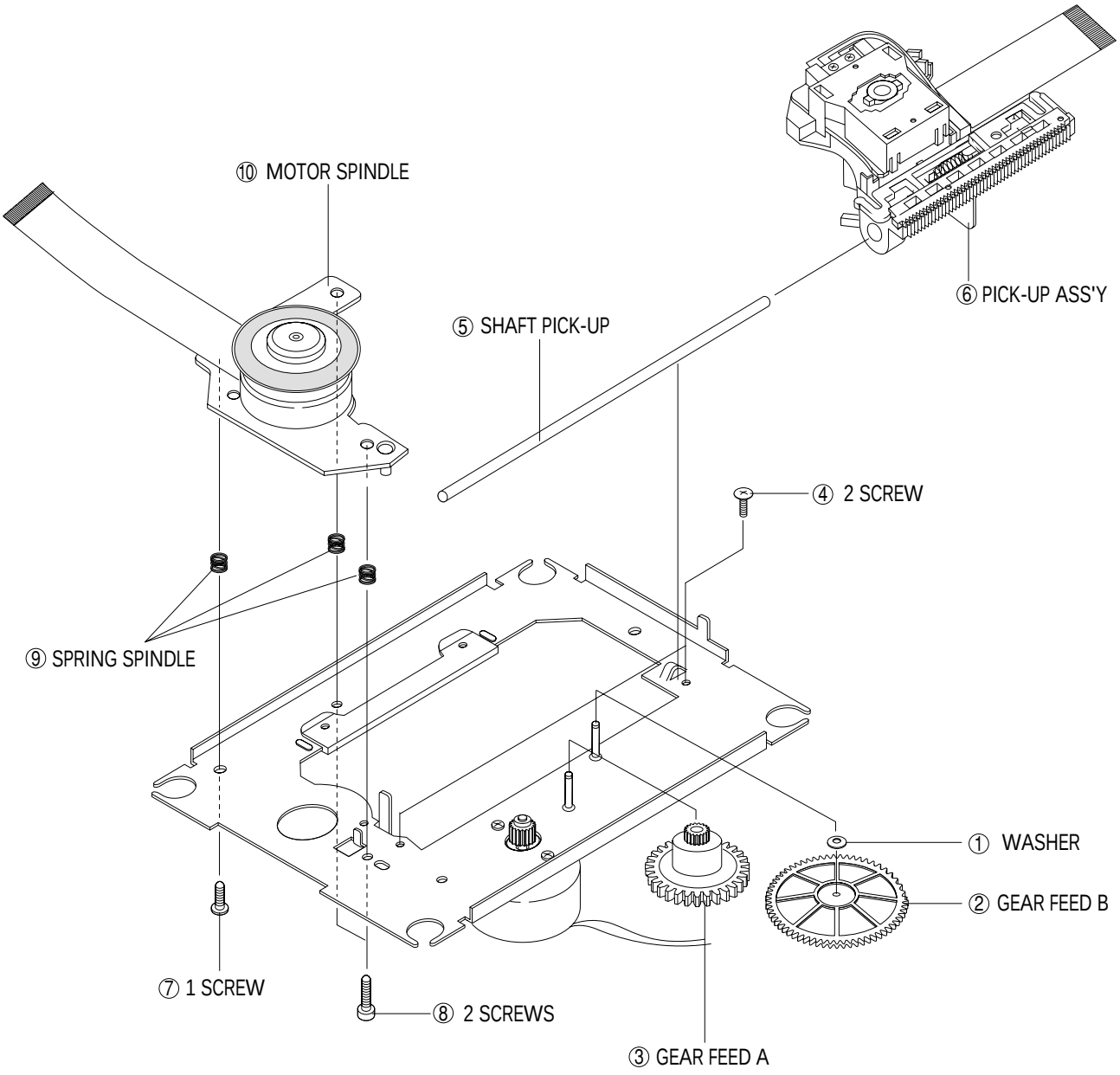


Fig. 5-13 Ass'y Brkt Deck Removal

MEMO

6. Circuit Descriptions

6-1 S.M.P.S.

6-1-1 Comparsion between Linear Power Supply and S.M.P.S.

6-1-1 (a) Linear

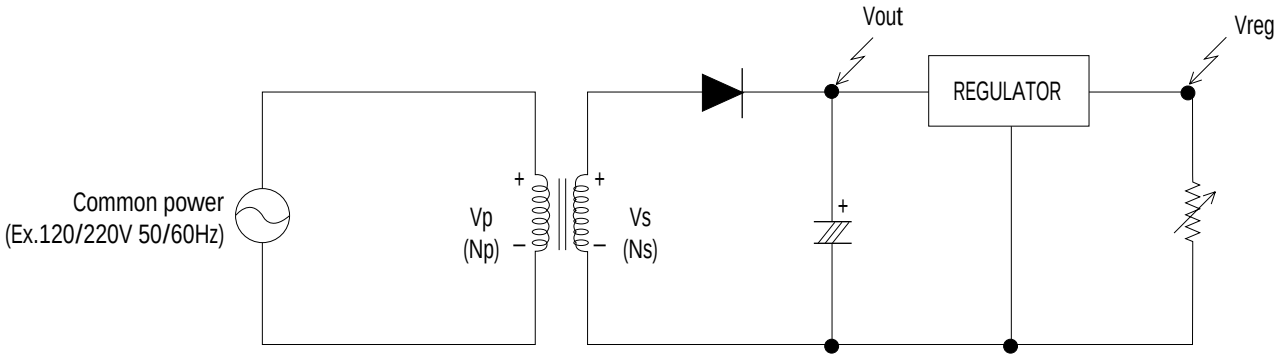


Fig. 6-1 Linear Power Supply

• Waveform/Description

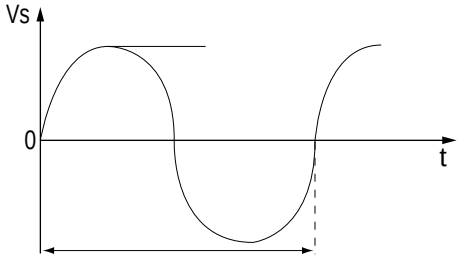


Fig. 6-2

Input : Common power to transformer (Vp).

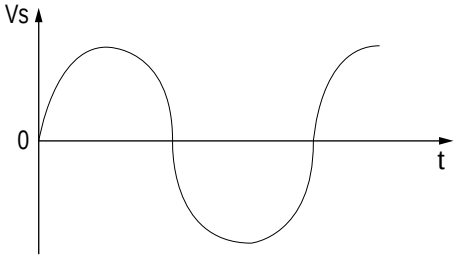


Fig. 6-3

The output Vs of transformer is determined by the ratio of 1st Np and 2nd Ns.
Vs = (Ns / Np) x Vp

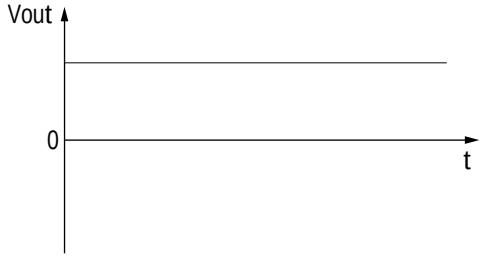


Fig. 6-4

Vout is output (DC) by diode and condensor.

• Advantages and disadvantages of linear power supply

1) Advantages : Little noise because the output waveform of transformer is sine wave.

2) Disadvantages :
① Additional margin is required because Vs is changed (depending on power source). (The regulator loss is caused by margin design).
② Greater core size and condensor capacity are needed, because the transformer works on a single power frequency.

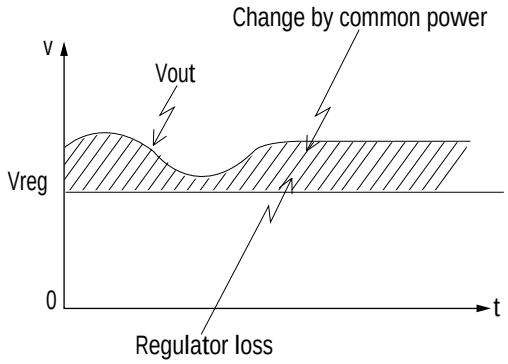


Fig. 6-5

6-1-1 (b) S.M.P.S. (Pulse width modulation method)

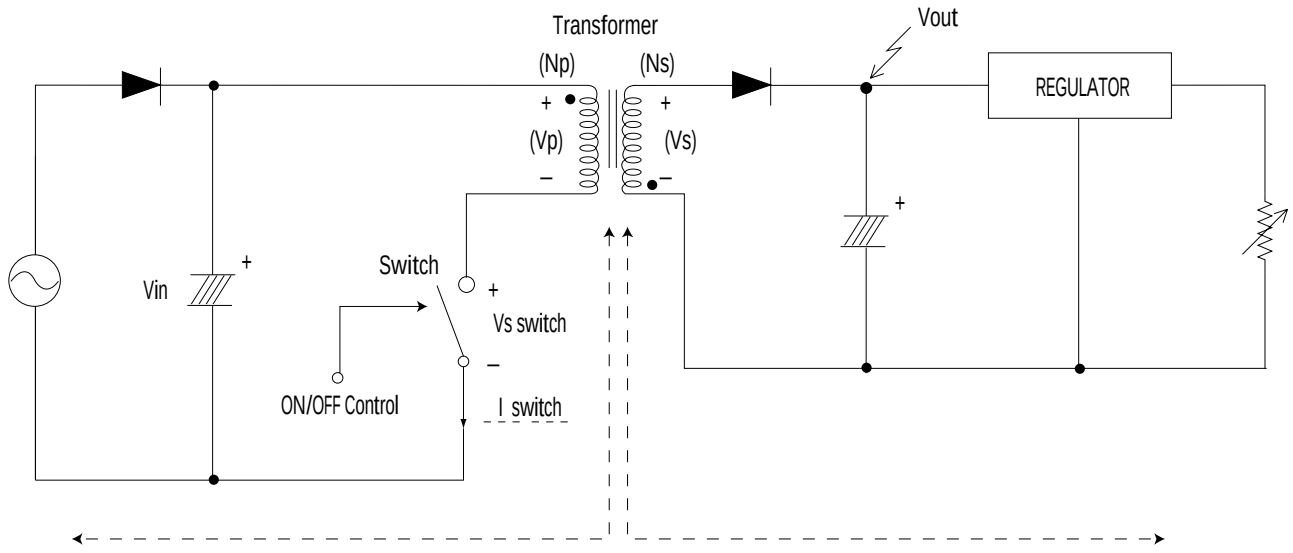


Fig. 6-6

• Terms

1) 1st : Common power input to 1st winding.
2) 2nd : Circuit followings output winding of transformer.
3) f (Frequency) : Switching frequency (T : Switching cycle)
4) Duty : (Ton / T) x 100

6-1-2 Circuit description (FLY-Back Control)

6-1-2 (a) AC Power Rectification/Smoothing Terminal

1) PDS01,PDS02,PDS03,PDS04 : Convert AC power to DC(Wave rectification).
2) PE3 : Smooth the voltage converted to DC.
3) PCR01, PCR02, PCD01, PCD02, PCD03, PLS01, PBS01 : Noise removal at power input/output.
4) PVA1 : SMPS protection at power surge input (PVA1 pattern open is to remove noise).

6-1-2 (b) SNUBBER Circuit : PER11, PDS11, PCR11, PCD12, PRS11, PRS12

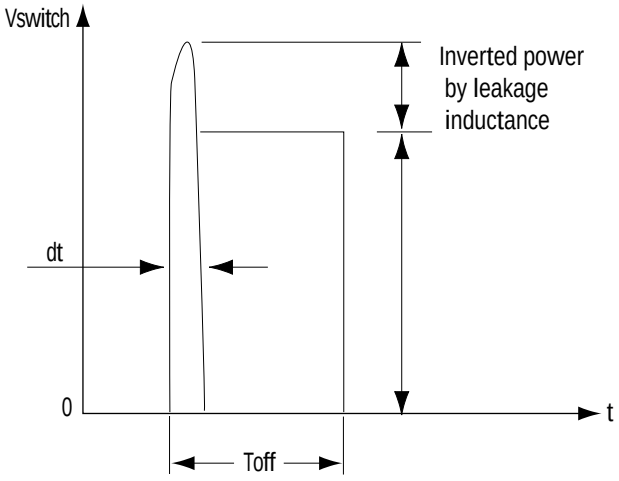


Fig. 6-7

1) Prevent residual high voltage at the terminals of switch during switch off/Suppress noise.
High inverted power occurs at switch (PIC1) off, because of the 1st winding of transformer :
(V= LI xdi/dt. LI : Leakage Induction)
A very high residual voltage exists on both terminals of PQR11 because dt is a very short.

2) SNUBBER circuit protects PIC1 from damage through leakage voltage suppression by RC, (Charges the leakage voltage to PER11, PDS11, PCR11, PCD12, and discharges to PR15 and PR16).

6-1-2 (c) Driving circuit

When Vin supplied, driving current Ig occurs throuhg the PRR11. By this IC (=HfexIg) occurs throug the PQR11 and the Vb is inducted to base winding coil NB of PQR11. By inducted Vb, Ib start flow and the PQR11 is saturated (S/W ON). Ib is constant and Ic increases in propotion to time. After constant time passed Ib become to shotage and PQR11 is cut OFF (S/W OFF).

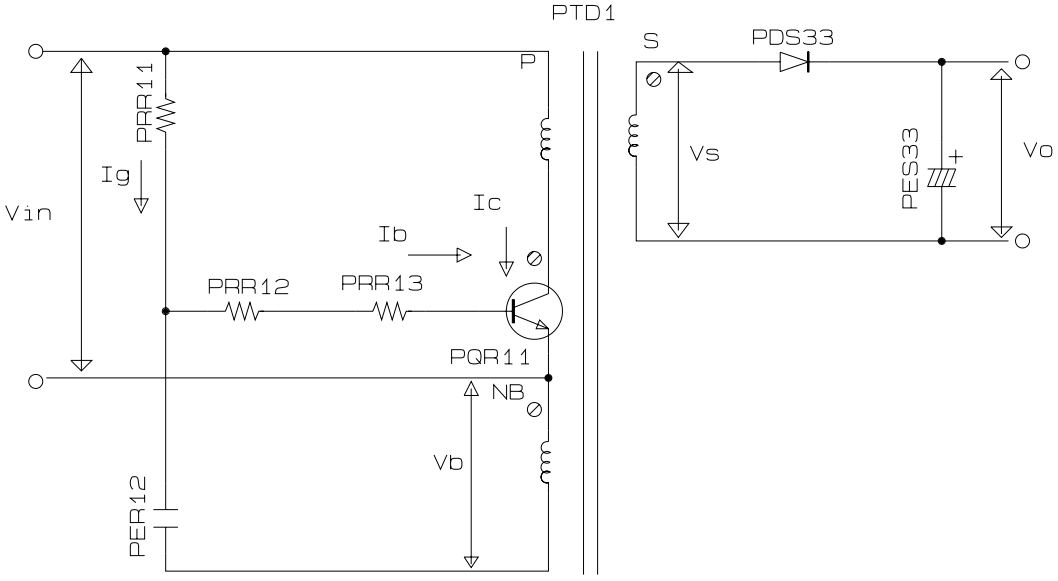


Fig. 6-8 Driving Circuit

6-1-2 (d) Feedback Control Circuit

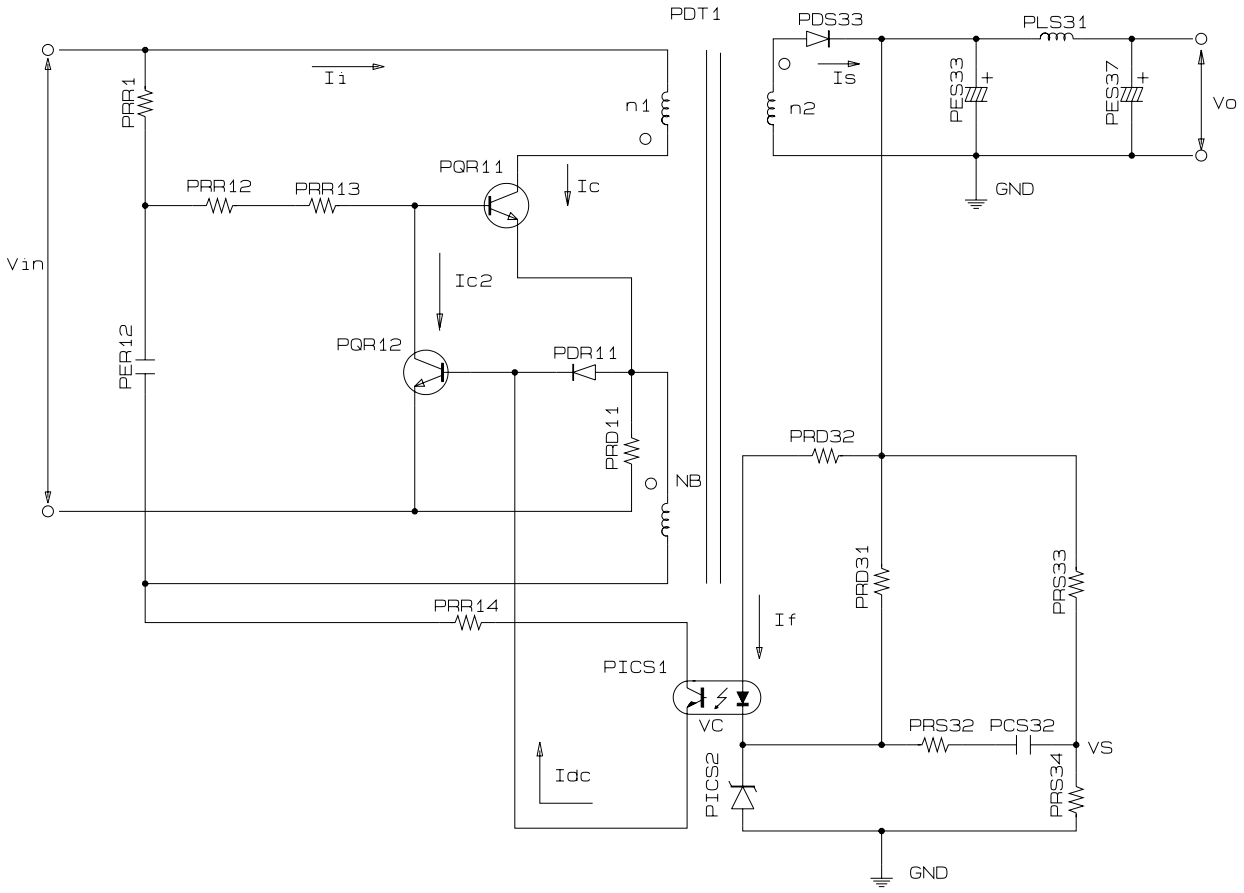


Fig. 6-9

• Operation descriptions

1) Internal OP-Amp '+' base potential of PICS2 is 2.5V and external "-" input potential is connected with PRS33 and PRS34 to maintain Vout of 5.8V.
2) If load of 5.8V terminal decreses (or AC inout voltage increases) and Vout increases over 5.8V,
   Then : PICS2 Vs potential up over 2.5V --> PICS2 Vc down --> PICS1 A-K potential down --> PICS1 C-E current up --> PQR12 base current up --> PQR11 base current down --> Vout down --> Maintain 5.8V

   - PRD31, PRD32 : Reduce 5.8V overshoot.
   - PRS32, PCS32 : Prevent PICS2 oscillation (for phase correction).

6-1-3 Internal Block Diagram

Internal Block Diagram

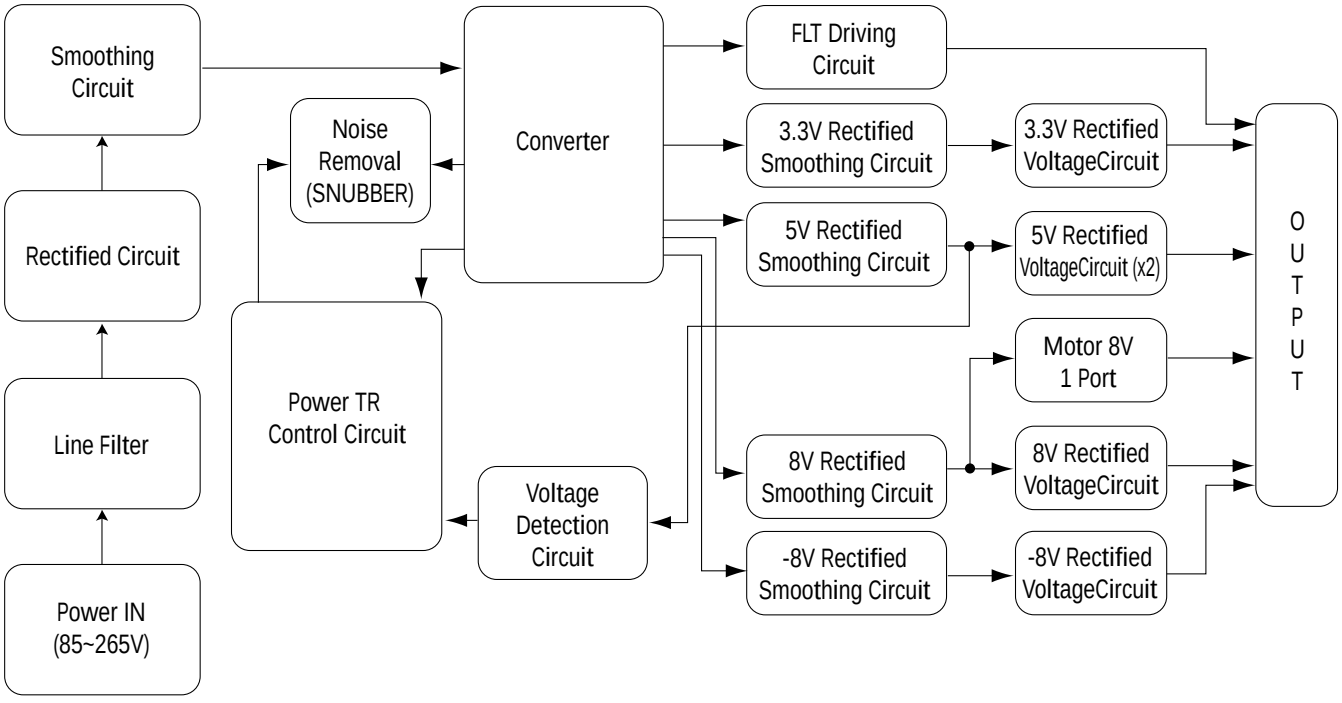


Fig. 6-10

6-2 RF

6-2-1 RIC1 (KS1461)

KS1461 is combined with KS1452 and KS1453 as bipolar IC developed for DVD SERVO system.
Main features include DVD waveform equalizing, CD waveform equalizing, focus error signal generation, 3-beam tracking error signal generation, DPD 1-beam tracking error, defect, envelope, MIRR output, etc. after receiving the pick-up output converted into I/V.

6-2-1 (a) Basic Potentiometer

KS1461 uses a single power method and each circuit is based on V of 2.5V.
V (Pin 12, 20, 24, 67) terminal is needed for IC, which uses the peripheral V.

6-2-1(b) RF signal

Fig. 6-11 shows the flow of signal generated by the pick-up.
A, B, C, D signals detected from pick-up are converted in to RF signal(A+B+C+D) via RF summing AMP.

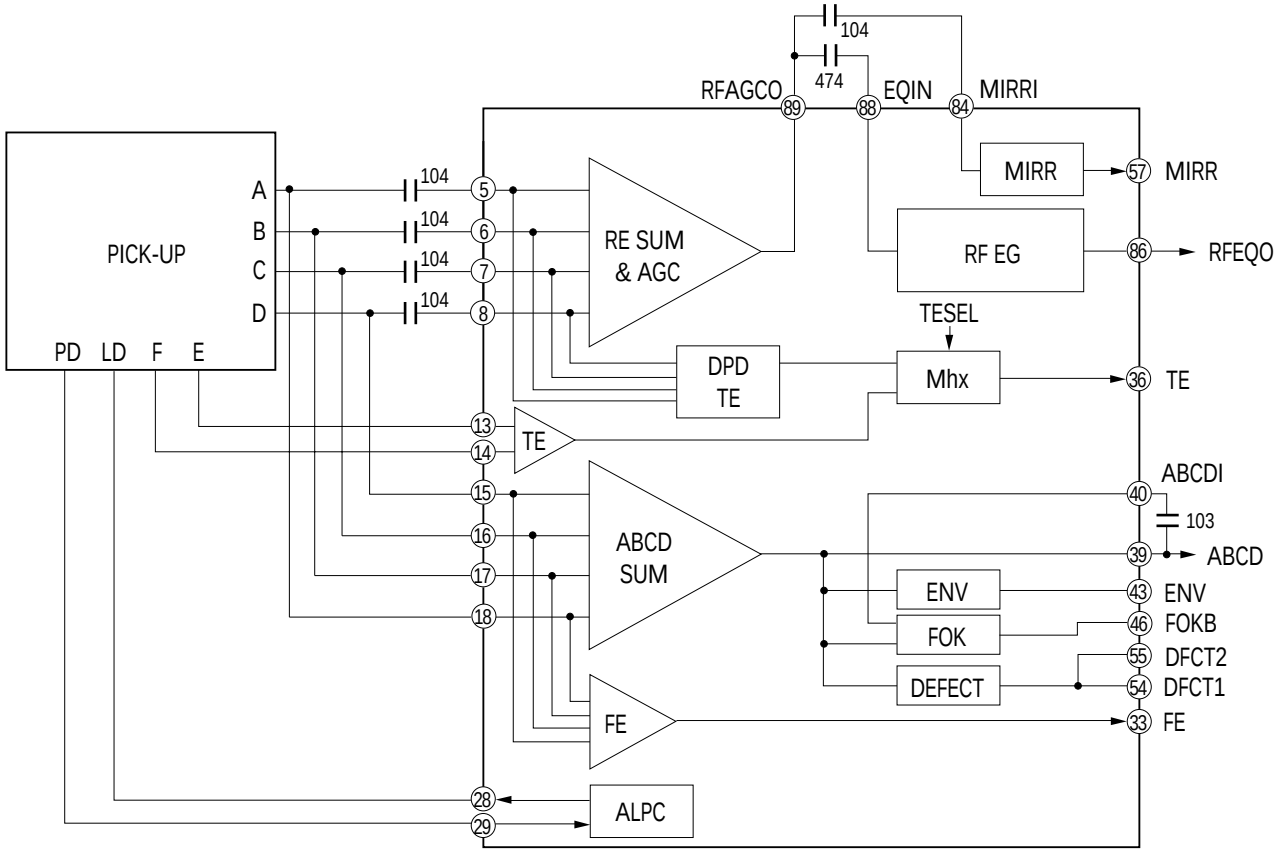


Fig. 6-11

Fig. 6-12 shows the waveform-equalizing block diagram for the RF signal.
It outputs to EQout (Pin 86) terminal by initially changing switching AMP gain of DVD and CD, and then adjusting the level in RF SUM & AGC. It controls RF SUM & AGC gain by means of Pin 89-95 and interfaces with PWM signal, (output from PWM terminal of KS1453, via low-pass filter to adjust boost gain and peak frequency.

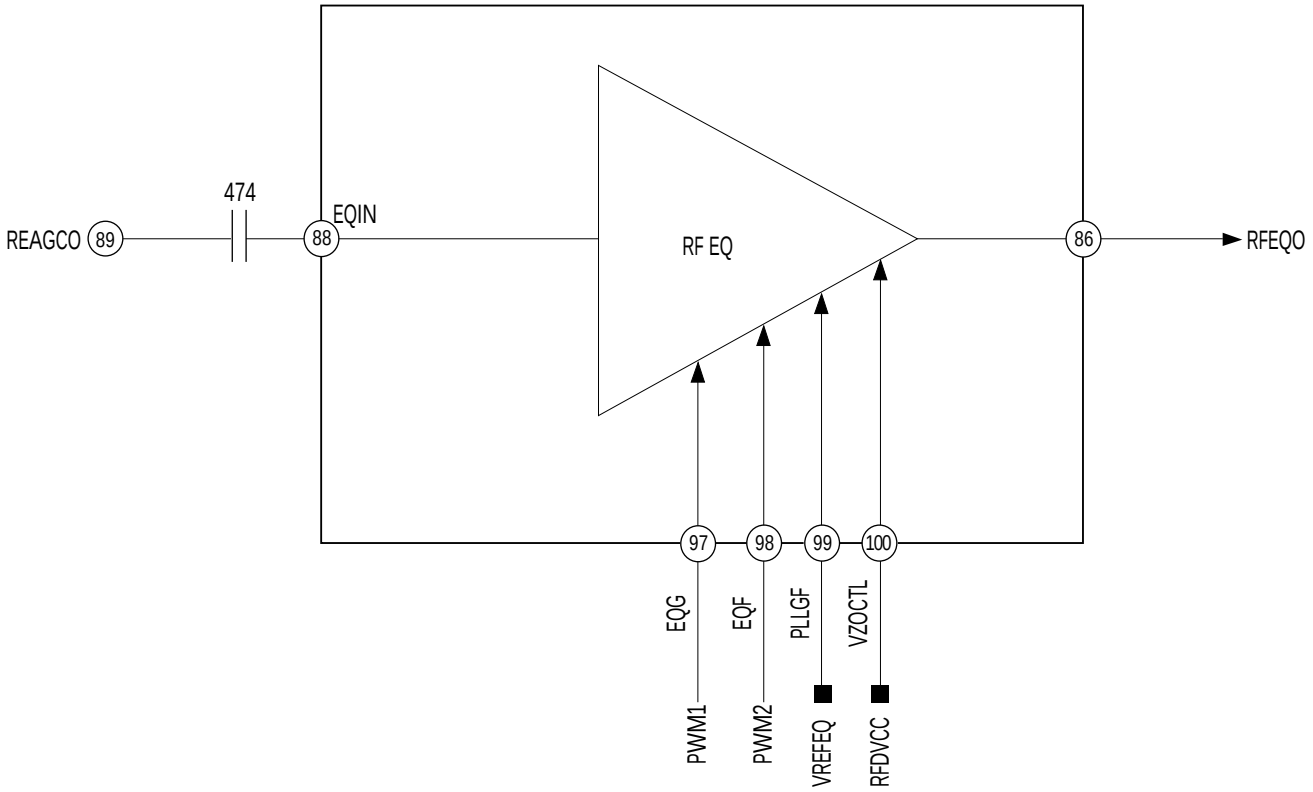


Fig. 6-12

The control parameters of DVD EQ and CD EQ are as follows.

1) DVD CD EQ control parameter

① EQG (Pin 97) : Changes the gain of peak frequency with EQ frequency characteristic. Convert PWM signal, output from KS1453, into DC via low-pass filter.

② EQF (Pin 98) : Changes the peak frequency with EQ frequency characteristic. Convert PWM signal, output from KS1453, into DVD via low-pass filter.

6-3 System Control

6-3-1 Outline

The main micom peripheral circuit is composed of 16bit Micom (MIC1 ; TMP95C265), 8M EPROM (MIC2 ; M27C801) for Microcode and data save, 256 byte EE-PROM (MIC4 ; KS24C020) for permanent storage of data needed at power off.
The Micom (MIC1 ; TMP95C265) mounted in main board analizes the key commands of front panel or instructions of remote control through communication with Micom (FIC1 ; LC86P6232) of front and controls the devices on board to execute the corresponding commands after initializing the devices connected with micom on board at power on.

6-3-2 Block Diagram

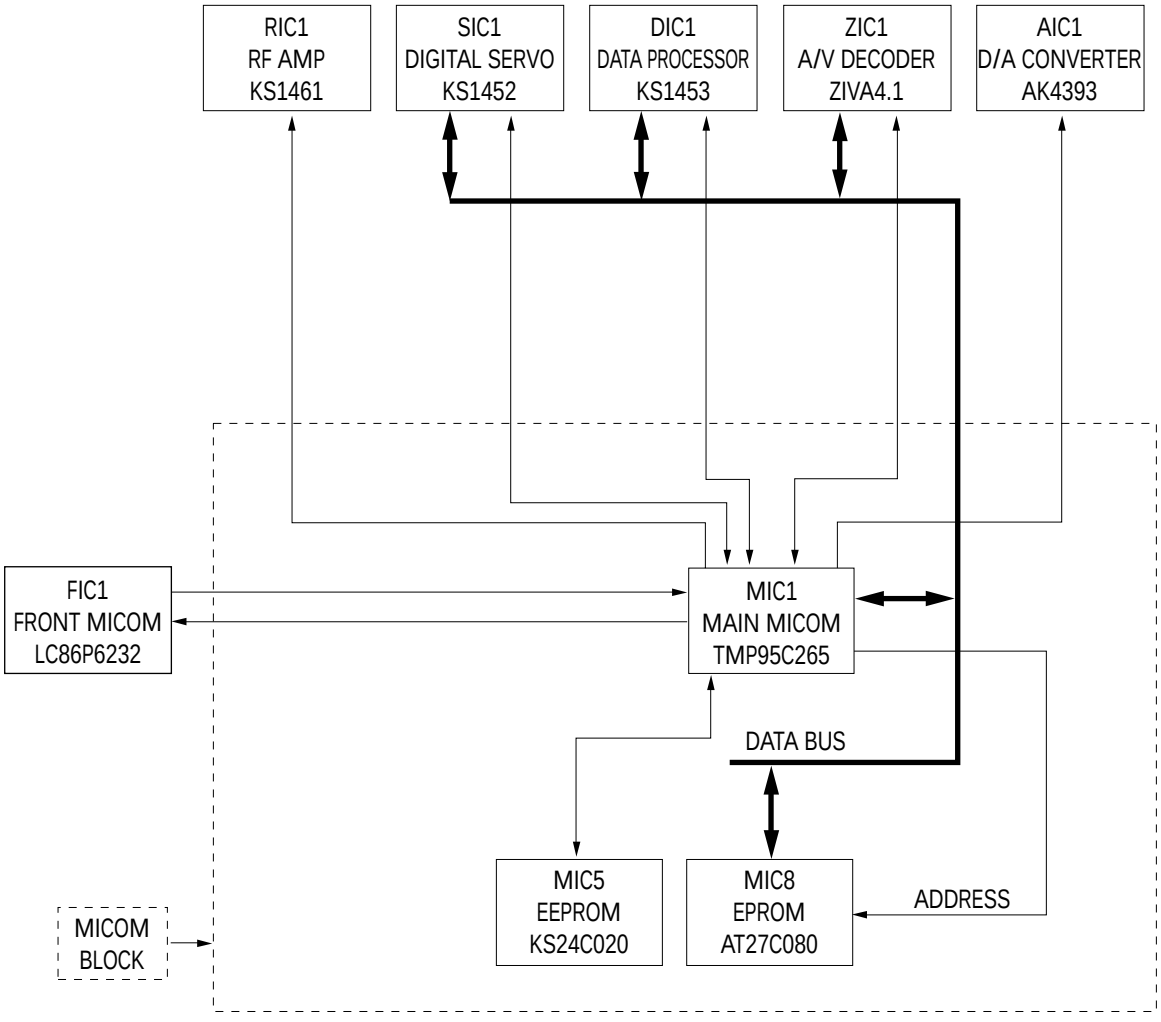


Fig. 6-13

6-3-3 Waveform Description

When micom accesses each device sharing bus, it falls the chip select signal of corresponding chip to (/CS1:MIC3-22, /CS2:MIC2-22, /DSPCS:DIC1-2, /DVD1CS:ZIC1-208, CSB:SIC1-10) 0 (Low) before trial.
So to speak, the bus is used by time-division as shown in Fig 6-14, 6-15, 6-16.
Two and more devices can't be accessed simultaneously.

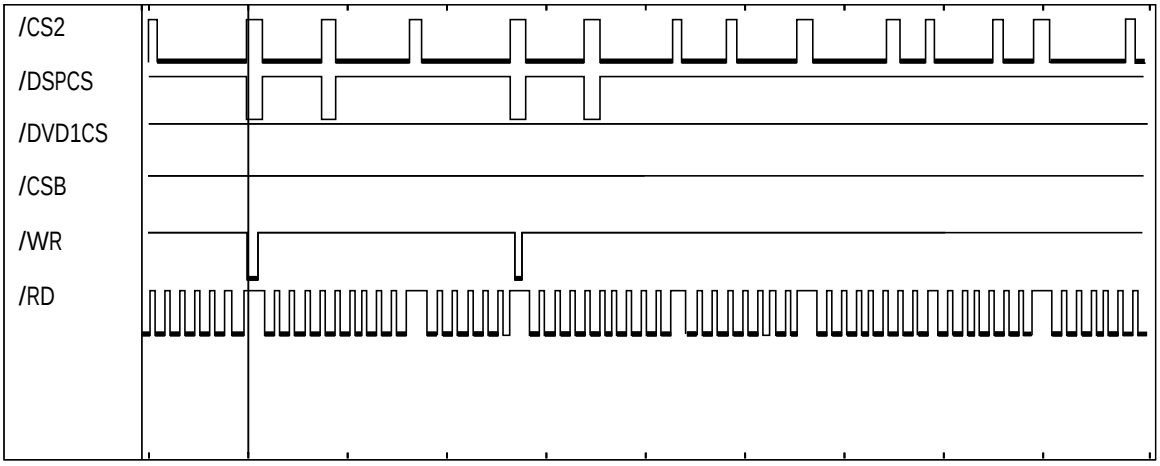


Fig. 6-14

- CH1 : CS2 (MIC2-22, EPROM CHIP SELECT)
- CH2 : DSPCS (DIC1-2, DATA PROCESSOR CHIP SELECT)
- CH3 : DVD1CS (ZIC1-208, A/V DECODER CHIP SELECT)
- CH4 : SRVCS (SIC1-10, DIGITAL SERVO CHIP SELECT)
- CH5 : WR (MIC1-89, MICOM OUTPUT WRITE SIGNAL)
- CH6 : RD (MIC1-88, MICOM OUTPUT READ SIGNAL)

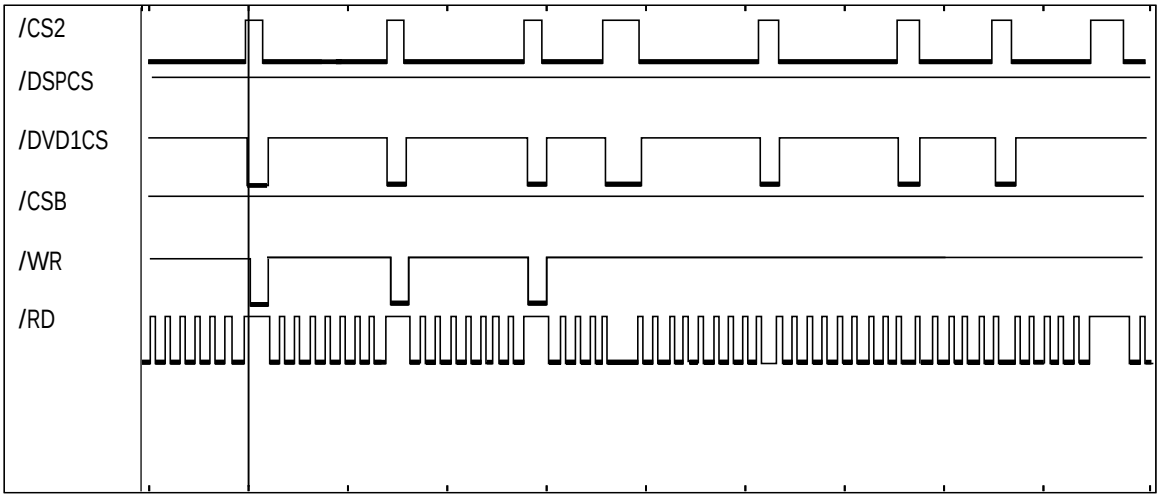


Fig. 6-15 DSP Access

- CH1 : CS2 (MIC2-22, EPROM CHIP SELECT)
- CH2 : DSPCS (DIC1-2, DATA PROCESSOR CHIP SELECT)
- CH3 : DVD1CS (ZIC1-208, A/V DECODER CHIP SELECT)
- CH4 : SRVCS (SIC1-10, DIGITAL SERVO CHIP SELECT)
- CH5 : WR (MIC1-89, MICOM OUTPUT WRITE SIGNAL)
- CH6 : RD (MIC1-88, MICOM OUTPUT READ SIGNAL)

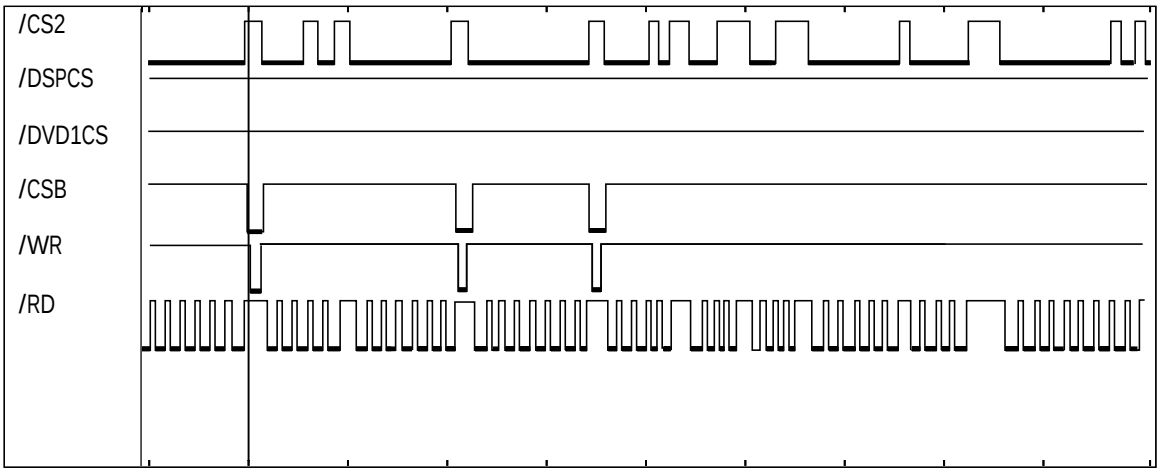


Fig. 6-16 Servo Access

- CH1 : CS2 (MIC2-22, EPROM CHIP SELECT)
- CH2 : DSPCS (DIC1-2, DATA PROCESSOR CHIP SELECT)
- CH3 : DVD1CS (ZIC1-208, A/V DECODER CHIP SELECT)
- CH4 : SRVCS (SIC1-10, DIGITAL SERVO CHIP SELECT)
- CH5 : WR (MIC1-89, MICOM OUTPUT WRITE SIGNAL)
- CH6 : RD (MIC1-88, MICOM OUTPUT READ SIGNAL)

6-4 Servo

6-4-1 Outline

SERVO system of DVD is divided into Focusing SERVO, Tracking SERVO, SLED Linked SERVO and CLV SERVO (DISC Motor Control SERVO).

1) Focusing SERVO
Focuses the optical spot output from object lens onto the disc surface. Maintains a uniform distance between object lens of Pick-up and disc (for surface vibration of disc).

2) Tracking SERVO
Make the object lens follow the disc track in use of tracking error signal (created from Pick-up).

3) SLED Linked SERVO
When the tracking actuator inclines outwardly as the object lens follows the track during play, the SLED motor moves slightly (and counteracts the incline).

4) CLV SERVO (DISC Motor Control SERVO)
Controls the disc motor to maintain a constant linear velocity (necessary for RF signal).

6-4-2 Block Diagram

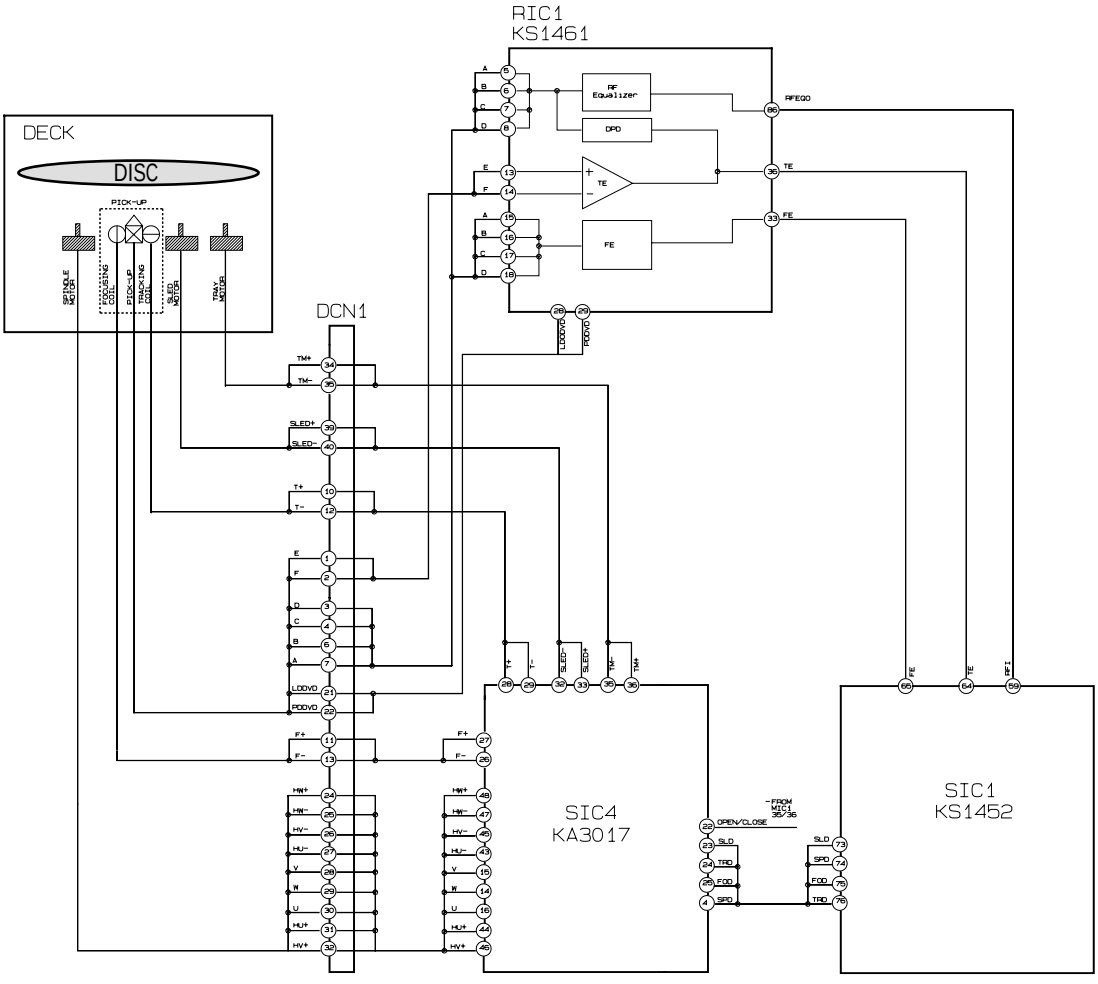


Fig. 6-17

6-4-3 Operation

1) FOCUSING SERVO

(1) FOCUS INPUT

The focus loop is changed from open loop to closed loop, and the triangular waveform moves the object lens up and down (at pin 75 of SIC1 during Focus SERVO ON.) At that time, S curve is input to pin 65 of SIC1.

ABAD (pin 39 of RIC1) signal, summing signal of PD A, B, C, D, is generated, and zero cross(2.5V) point occurs when S curve is focused and ABAD signal exceeds a preset,constant value. The focus loop is changed to closed loop, and the object lens follows the disc movement, maintaining a constant distance from the disc. (these operations are same in CD and DVD).

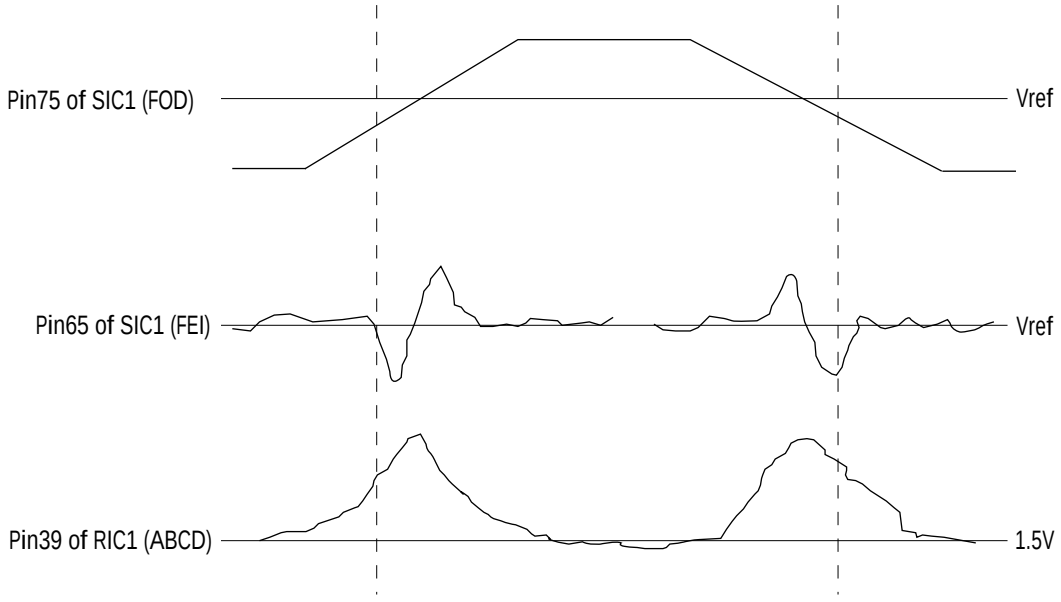


Fig. 6-18

(2) PLAY

When focus loop closes the loop during focus servo on, both pin 65 and pin 75 of SIC1 are controlled by VREF voltage (approx. 2.5V), and pin 26, 27 of SIC4 are approximately 4.5V.

2) TRACKING SERVO

(1) NORMAL PLAY MODE

① For DVD

Composite : The signal output from PD A, B, C, D of Pick-up, the tracking error signal (pin36 of RIC1) uses the phase difference of A+C and B+D in RIC1, and inputs to terminal 64 of SIC1. Then, it is output to SIC1 pin 76 via digital equalizer, and applied to the tracking actuator through SIC4.

Pins 76 of SIC1 is controlled by VREF(approx. 2.5V) during normal play.

Meanwhile, DVD repeats the track jump from 1 to 4 in inner direction at normal play (because data- read speed from disc is faster than data output speed on screen).

② For CD, VCD

Receive the signal output through E, F of Pick-up, from RIC1. The tracking error signal is similar to DVD.

(2) SEARCH Mode :

Search mode : Fine seek,(Moving the tracking actuator slightly little below 255 track) and coarse search, moving much in use of sled motor. The coarse search will be described in sled linked servo and now, the fine seek is explained shortly.
If the object lens is located near target, cut off the tracking loop and give the control signal as many as desired count to move the tracking actuator via SIC1 pin 76 terminal(TRD).

3) SLED LINKED SERVO

· Normal play mode
Move SLED motor slightly by means of PWM signal in SIC1 pin 73, as the tracking actuator moves along with track during play. Control to move the entire Pick-up as the tracking actuator moves.

· Coarse serach mode
In case of long-distance search (such as chapter serach), SIC1 uses MIRR and TZC signal of SIC1-38, 52.
Then, read ID and compute the existing track count after input of next
track. If the existing track count is within fine seek range, tracking begins using fine seek.

4) CLV SERVO(DISC MOTOR CONTROL SERVO)

Input RF signal (from Pick-up) to SIC1 pin59. Detect SYNC signal from RF in SIC1, and output PWM signal to SIC1 pin 55 for constant linear velocity.

6-5 DVD Data Processor

6-5-1 Outline

DIC1(KS1453) performs Sync detection, EFM demodulation and error correction and Spindle motor control (CLV control) after inputting sliced EFM signal of RF signal at disc playback and EFM read clock (PLCK) signal generated from PLL. Outputs data which converted to the last audio and video from A/V decoder (ZIC1). KS1453 uses external memory(4M DRAM) as buffer as well as for error correction and carries out Variable Bit Rate transfer function. VBR function uses the external buffer as buffer to absorb the difference of transfer rate occurring because the transfer rate of disc playback is faster than data transfer rate demanded by A/V decoder(Video/Audio Signal Process Chip).
In case of general disc refresh, the memory is almost filled up periodically. It is because Write rate to memory after disc playback and signal process is faster than Read of A/V decoder. When the memory is filled, this status is reported by interrupt to main micom, which controls the servo to kick back the pick-up to the previous track after memorizing the last data read from disc until now. It takes some times to jump to the previous track and return to the original(jump location) again. The memory will have an empty space because A/V decoder reads out data of memory.
When the memory has an empty space, where data can be processed and written and the pick-up correctly gets to the original location(before kick back location) again, it reads data again avoids the interrupt of data read previously. The basic operation repeats to perform as described above.

6-5-2 Block Diagram

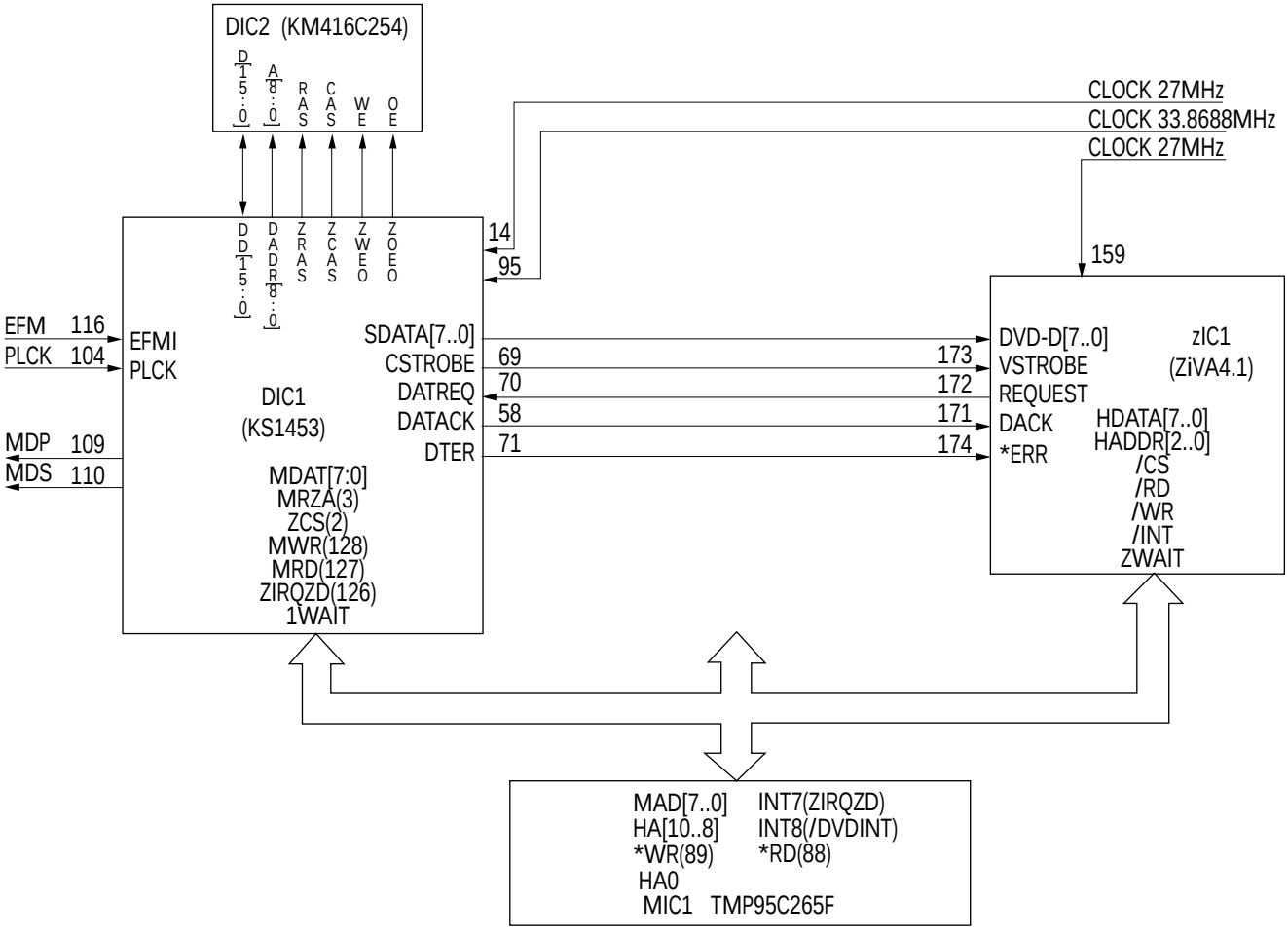


Fig. 6-19

6-5-3 Waveform Description

It measures the timing that data processed in DIC1 at DVD playback.

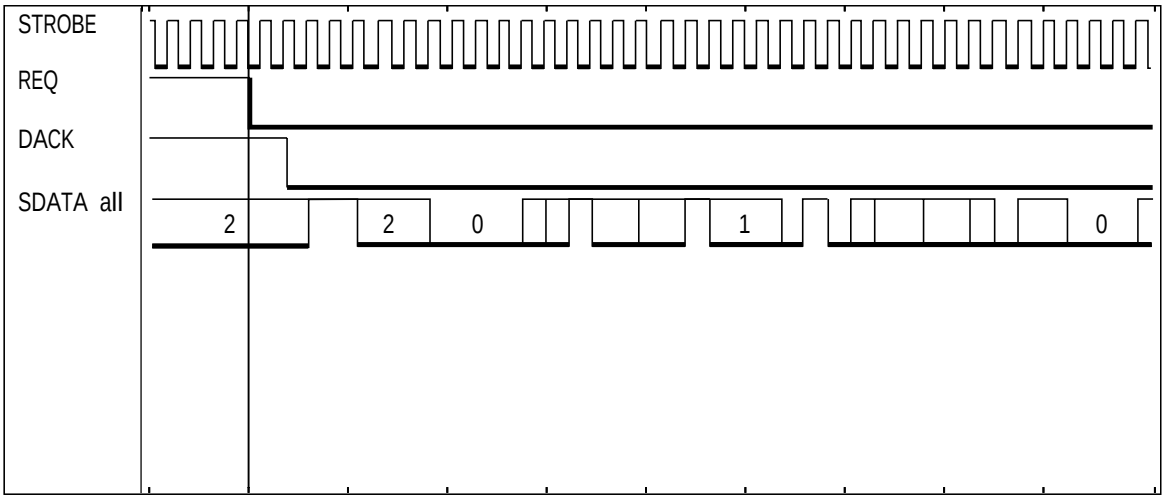


Fig. 6-20

- CH1 : STROBE (DIC1-69, CLOCK)
- CH2 : REQ (DIC1-70, DATA REQUEST)
- CH3 : DACK (DIC1-58, DATA ACKNOWLEDGE)
- CH4 : SDATA (DIC1-60~67, DATA)

6-6 Video

6-6-1 Outline

ZIC1(A / V decoder with video encoder) diverges from the 27MHz crystal, then generates VHSYNC and HSYNC.
ZIC1(A / V decoder with video encoder) does RGB encoding,copy guard processing and D / A conversion of 8bit video data internally inputted from video decoder block by MIC1(Micom).
Video signal converted into analog signal is outputted via amplifier of analog part.

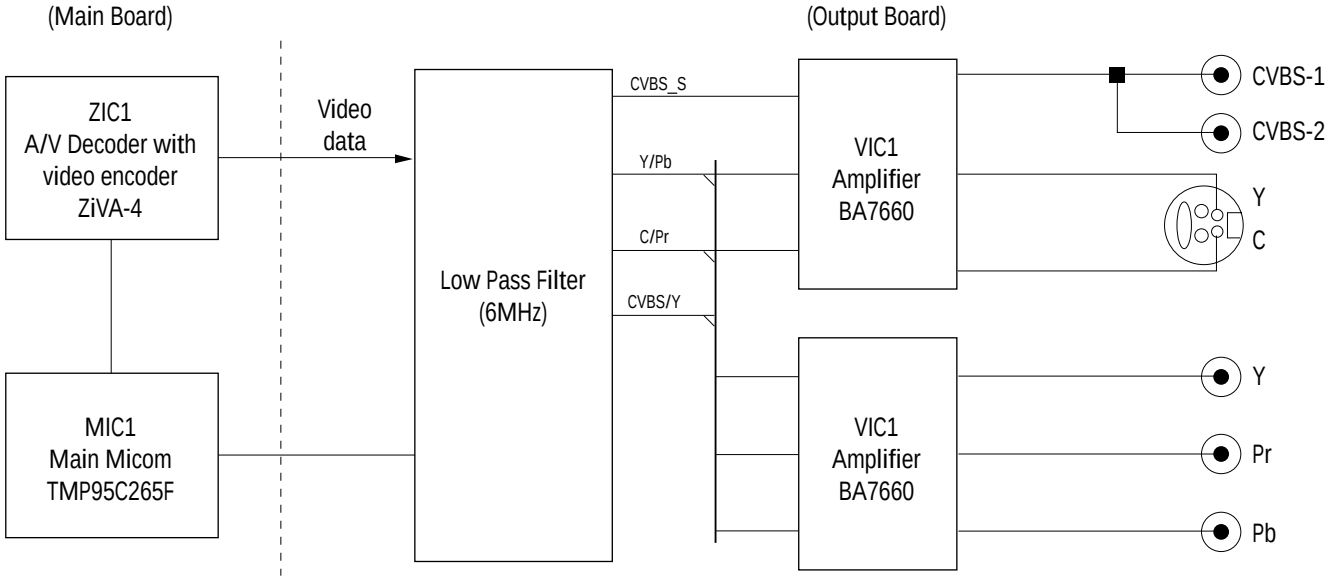


Fig. 6-21 Video Output Block Diagram

6-6-2 NTSC Digital Encoder (ZIVA-4.1 ; Buit in video encode)

ZIC1 inputted from pin159 with 27MHz generates HSYNC and VSYNC which are based on video signal.
ZIC1 is synchronous signals with decoded video signal and control the output timing of 8bit video signal of ITU-R601 format.
The inputted 8bit data which decoded from video decoder block is demuxed with each 8bit of Y, R-Y, B-Y. The separate signal is encoded to NTSC by control of MIC1.
The above signals, which are CVBS(Composite Video Burst Synchronized) / G(GREEN) / Y[PIN139], Y(S_VIDEO) / B(BRUE) / Pb[PIN145] and C(S_VIDEO) / R(RED) / Pr[PIN151], are selectively outputted CVBS +S_VIDEO, Y+Pr+Pb by the rear switch.
In Course of encoding,8bit data can extend to 10bit or more. To convert the extended data to quantization noise as possible,ZIC1 adopts 10bit D / A converter. ZIC1 perform video en-coding as well as copy protection.

6-6-3 Amplifier (VIC1, VIC2 : BA7660)

VIC1 and VIC2 are 6dB amplifier. Based on CVBS signal, the final output level must be 2Vpp without 75ohm terminal resitance. Because the level of video encoder output is only 1.1Vpp, the level is adjusted with the special amplifier. When mute of pin 1 is high active, if the pin is floating and connecte to power, the output isgnal is never outputted. CVBS,Y,C,Y,Cr,Cb outputted from video encoder are inputted to VIC1(Pin 7,Pin2,Pin4),and VIC2(Pin7,Pin4,Pin2) respectively and outputted from VIC1(Pin15,Pin13,Pin10) and VIC2(Pin15,Pin13,Pin10). Pin9, Pin12, Pin14 of VIC1, VIC2 are feedback pin to SAG compensation(DC characteristic compensation of siganl).
The signal to which gain is adjusted by amplifier is outputted from jack via 75ohm Resistance(VR10~VR13, VR22~24).

6-7 Audio

6-7-1 Outline

The four data (Data 0~3) outputted from A / V decoder (ZIC1 ; ZiVA4.1) are supplied to DATA 0 for 2-channel mixed audio output and to DATA 1~3 for Analog audio output (5.1-channel).
The audio data (0~3) transmitted from A / V decoder (ZIC1 ; ZiVA4.1) are converted into analog signal via audio D / A converter and outputted via post filter and amplifier.
CD and VCD are outputted with only 2 channels audio data and transmit them to Data 0 and Data 1.
Front L / R channel is outputted in mixed audio output (L / R output) and analog audio output and surround L / R, center and subwoofer aren't outputted.
If DVD of 2 channels source disc is used, it is outputted by the same way with CD and VCD.
If 5.1-channel source disc, front L / R channel is outputted in Data 1, Surround L / R in Data 2 and Center / Sub-woofer in Data 3. At that time, 5.1 channel can be downmixed in 2 channel in Data 0.

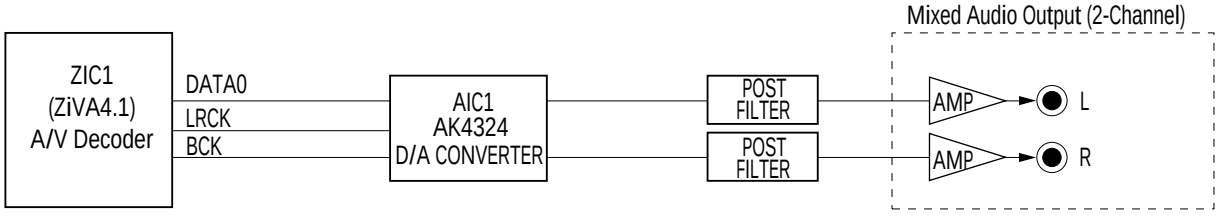


Fig. 6-22 Audio Output Block Diagram

6-7-2 DVD Audio Output

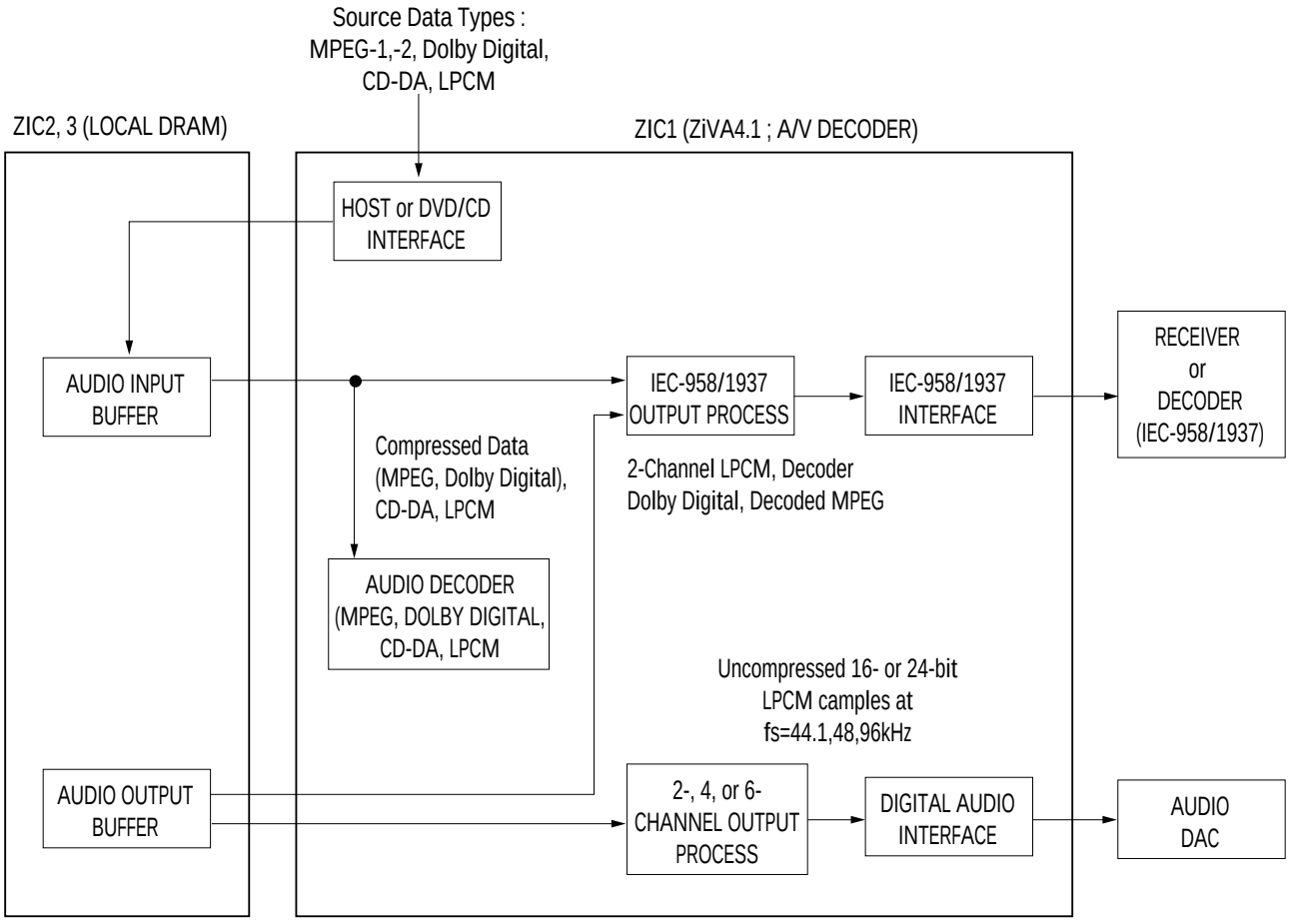


Fig. 6-23 Audio Decoder and Output Interface Datapath

1) Compressed Data

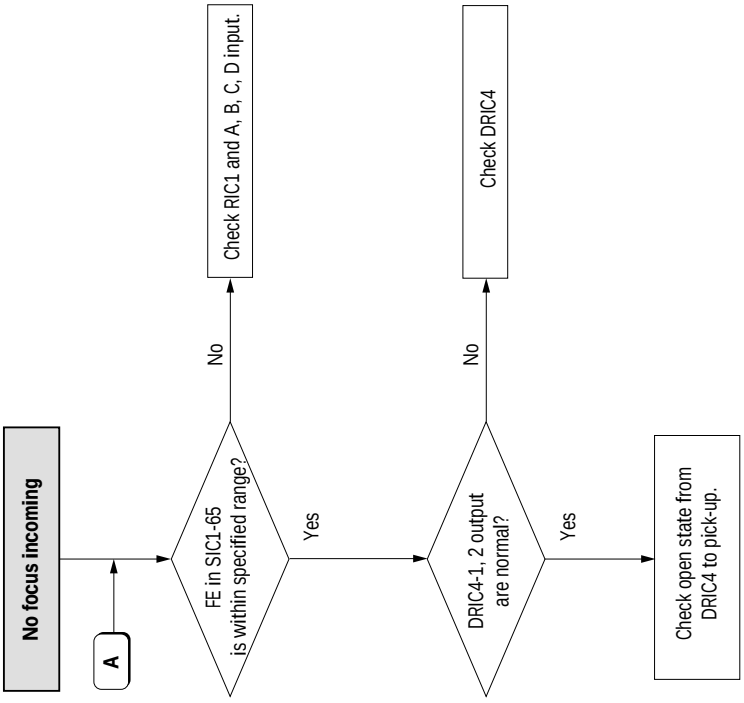
The audio data inputted to ZIC1 (ZiVA4.1) A / V decoder is divided into compressed data and uncompressed data. It is compressed data that is compressed with multi-channel audio data such as Dolby digital, MPEG, DTS, etc. The compressed data inputted to ZIC1 (ZiVA4.1) is converted into the uncompressed data of 2, 4, and 6 channels through ZiVA4.1 built-in audio decoder and is outputted to Data 0, 1, 2, and 3 through digital audio interface. The compressed data is transmitted to external AC-3 amplifier or MPEG / DTS amplifier as IEC-958 / 1937 transmission data format compressed by ZiVA4.1 built-in IEC-958 output process.

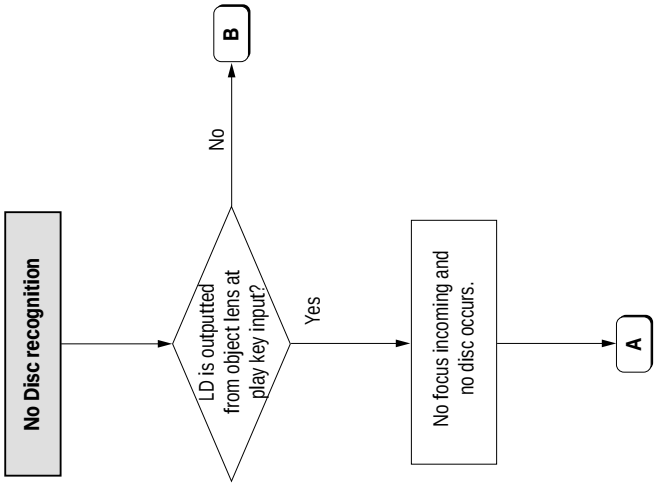
2) Uncompressed Data

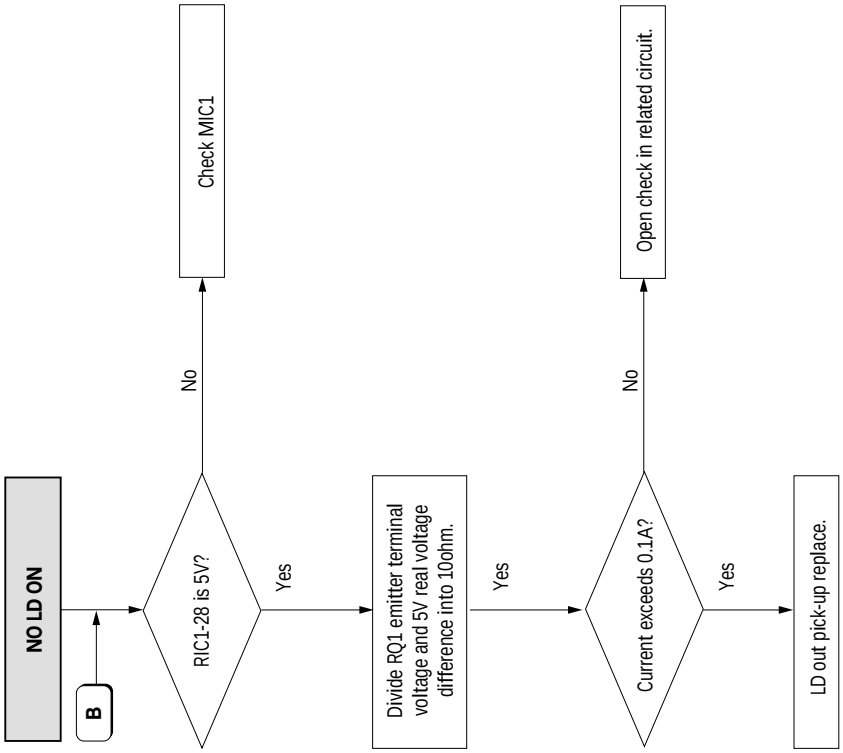
The uncompressed data is that data isn't compressed, so it is called CD-DA, LPCM data.
The 2 channels data is converted through audio decoder 2-channel data and Data 0 and Data 1 are outputted in digital audio interface.Via IEC-958 output process, they is transmitted to digital amplifier or AC-3 / MPEG / DTS amplifier built in the external digital input source with IEC-958 / 1937 transmission format.

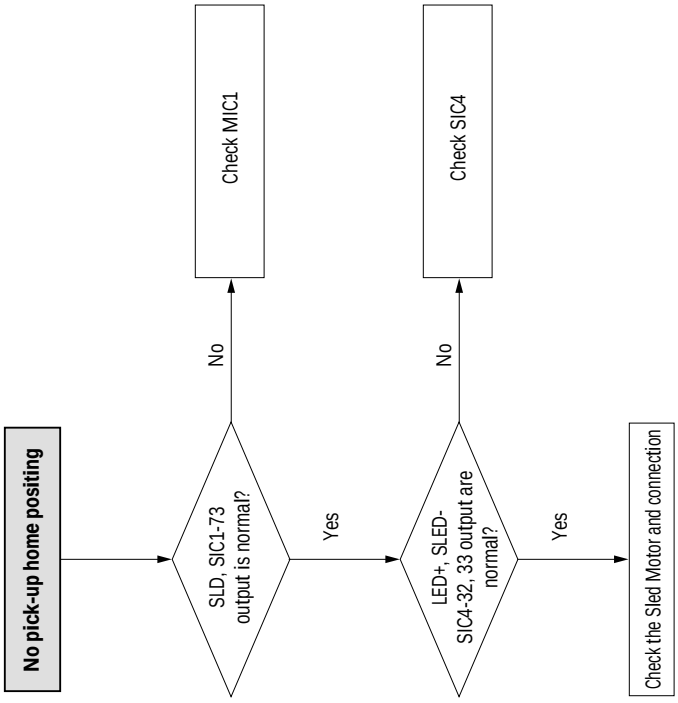
MEMO

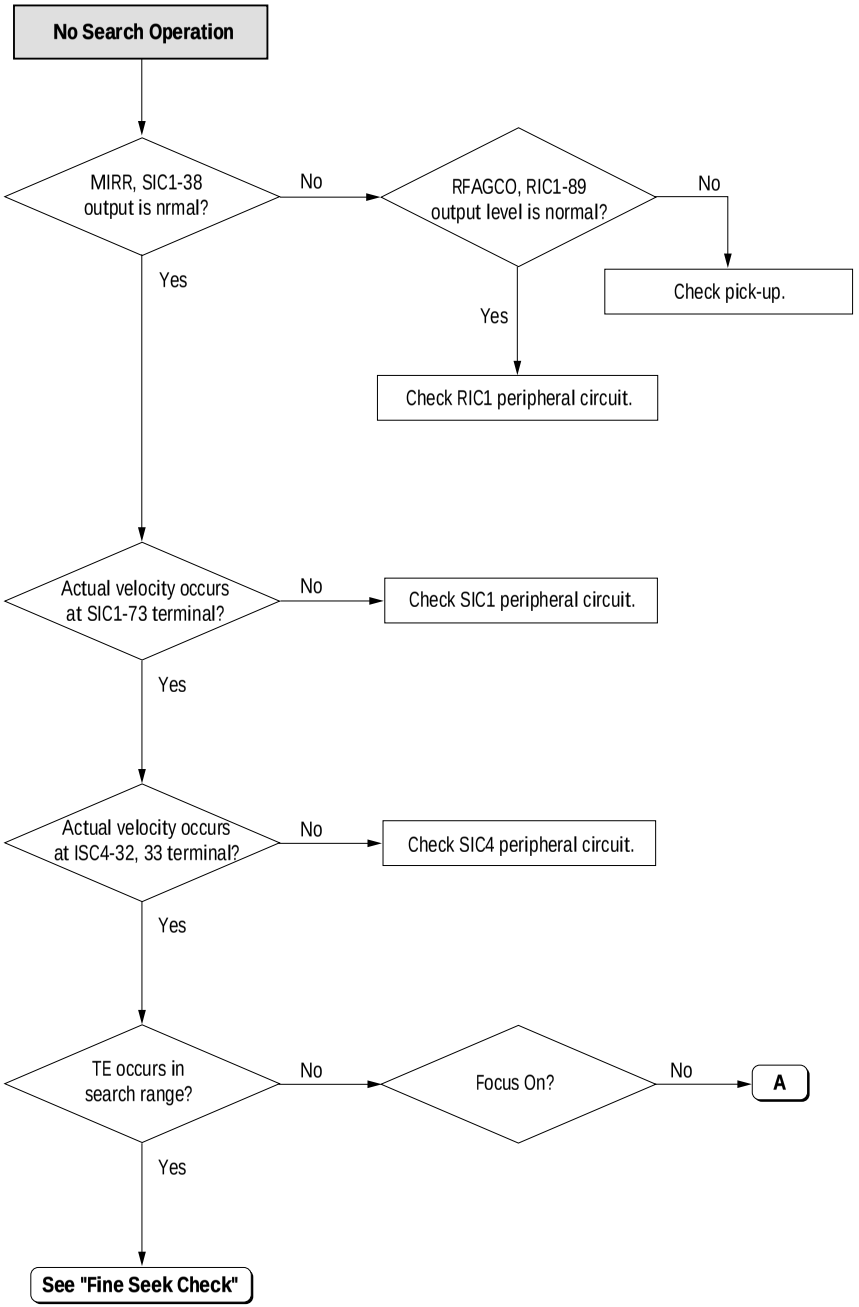
7. Troubleshooting

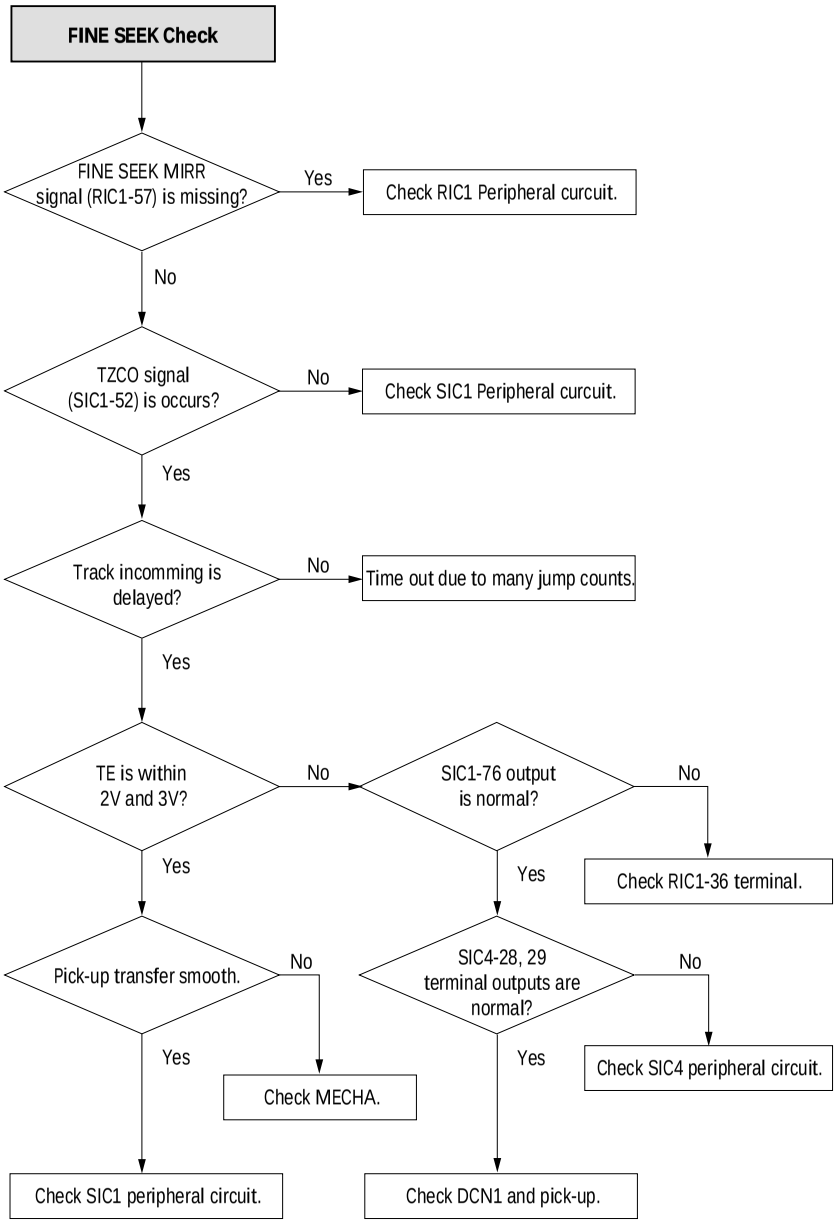


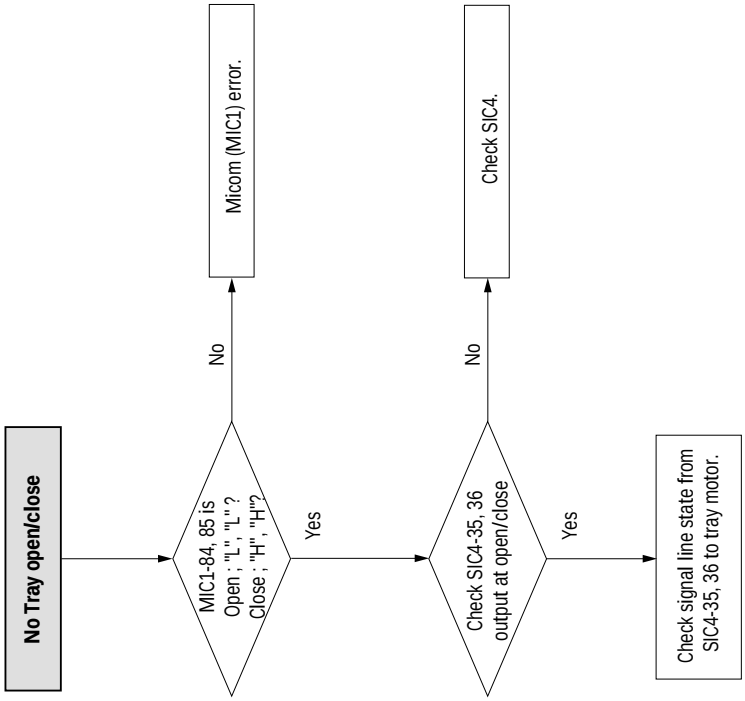


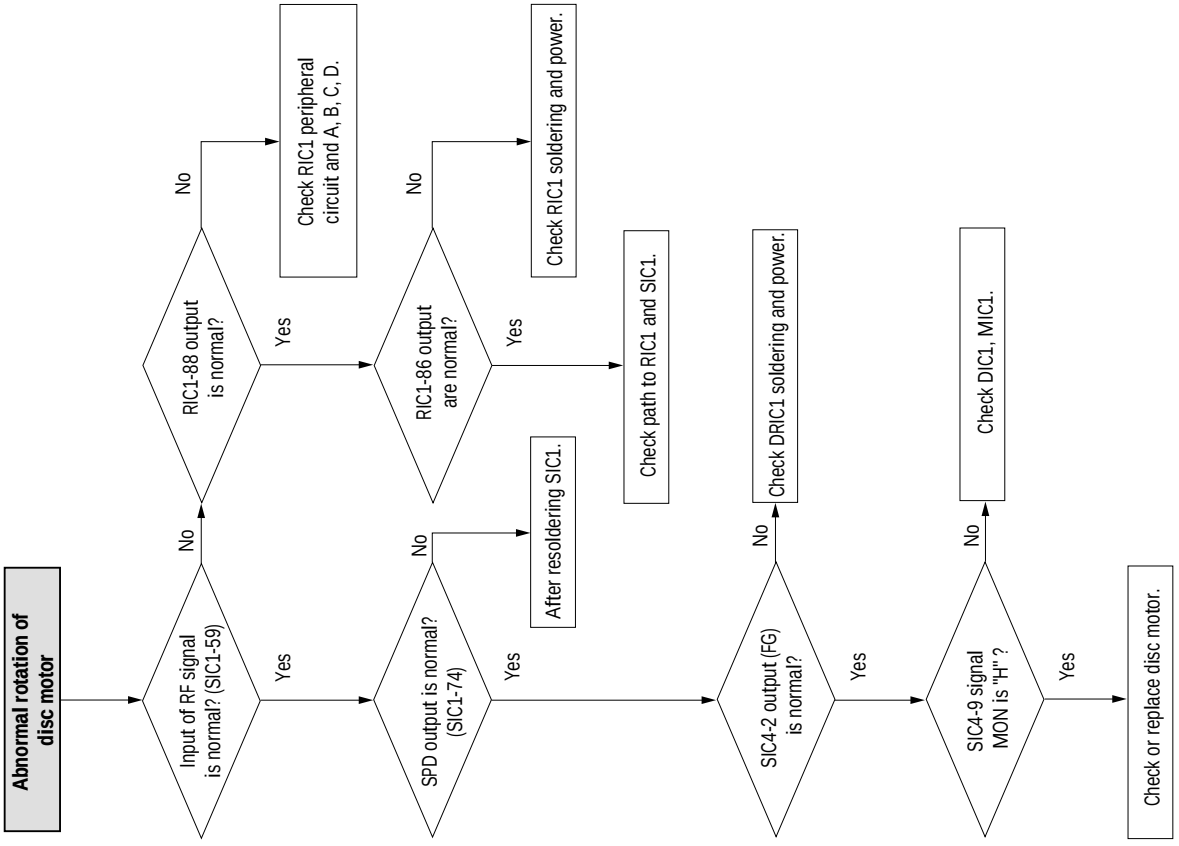

NO LD ON
B
RIC1-28 is 5V?
No
Check MIC1
Yes
Divide RQ1 emitter terminal voltage and 5V real voltage difference into 10ohm.
Yes
Current exceeds 0.1A?
No
Open check in related circuit.
Yes
LD out pick-up replace.

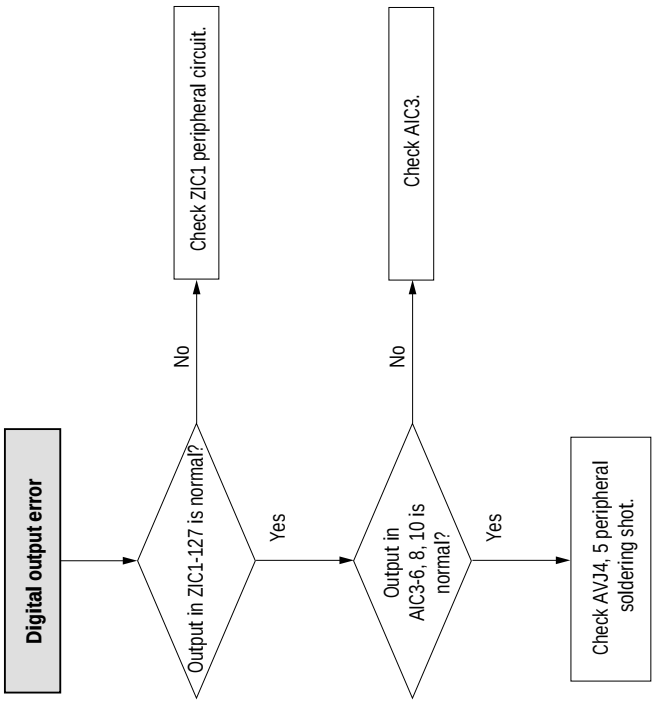

No pick-up home positing
SLD, SIC1-73 output is normal?
No
Check MIC1
Yes
LED+, SLED- SIC4-32, 33 output are normal?
No
Check SIC4
Yes
Check the Sled Motor and connection

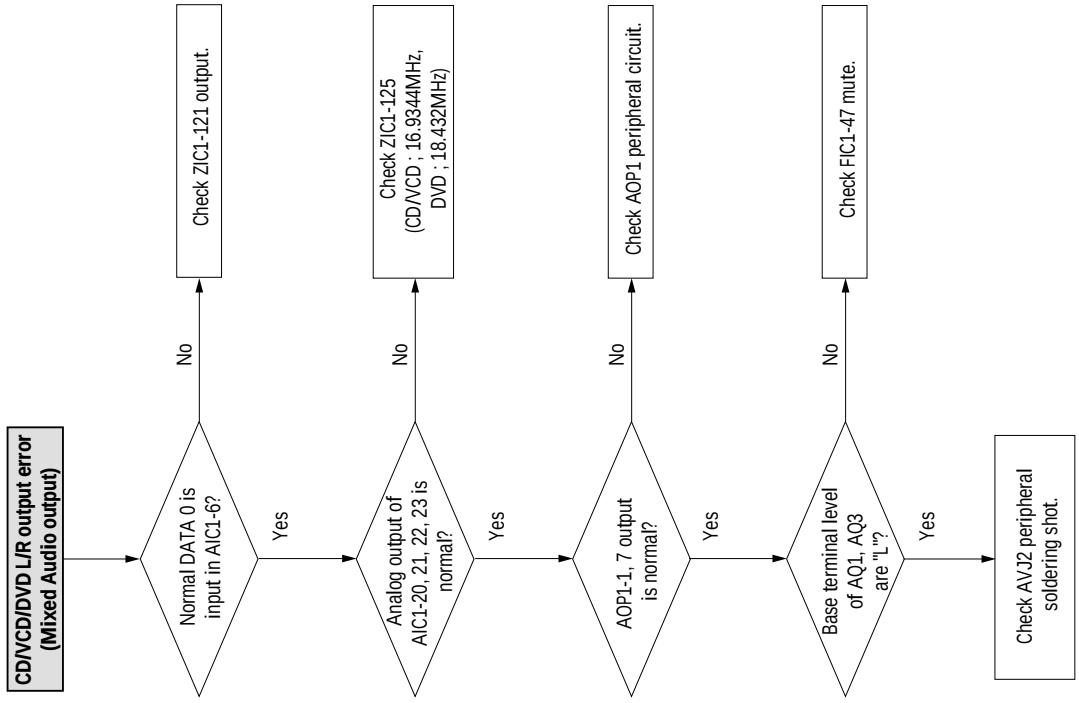

No Search Operation
MIRR, SIC1-38 output is nrmal?
No
RFAGCO, RIC1-89 output level is normal?
No
Check pick-up.
Yes
Check RIC1 peripheral circuit.
Yes
Actual velocity occurs at SIC1-73 terminal?
No
Check SIC1 peripheral circuit.
Yes
Actual velocity occurs at ISC4-32, 33 terminal?
No
Check SIC4 peripheral circuit.
Yes
TE occurs in search range?
No
Focus On?
No
A
Yes
See "Fine Seek Check"

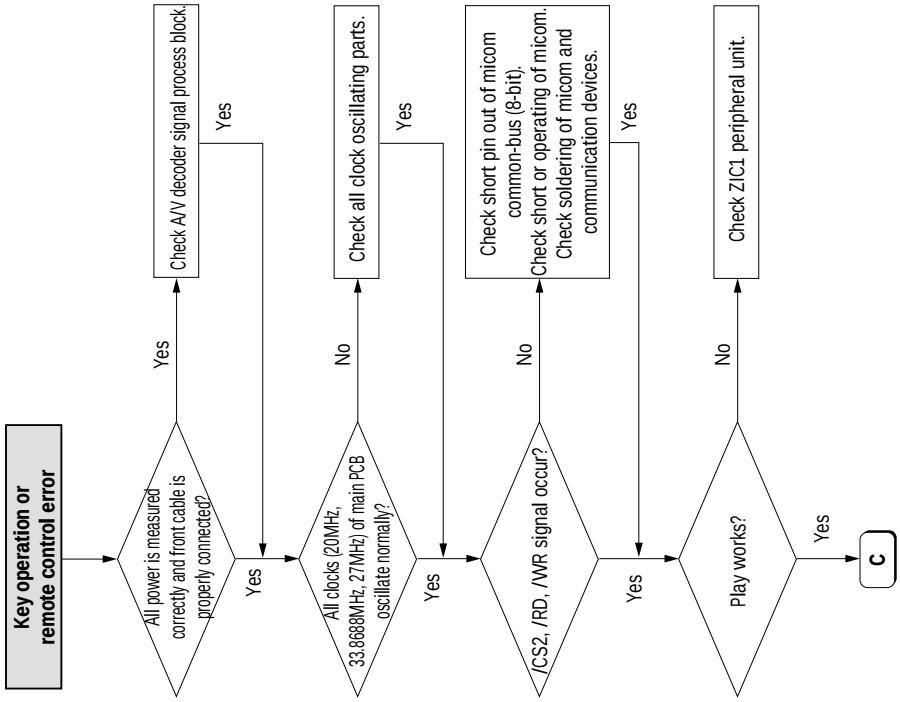

FINE SEEK Check
FINE SEEK MIRR signal (RIC1-57) is missing?
Yes
Check RIC1 Peripheral curcuit.
No
TZCO signal (SIC1-52) is occurs?
No
Check SIC1 Peripheral curcuit.
Yes
Track incomming is delayed?
No
Time out due to many jump counts.
Yes
TE is within 2V and 3V?
No
SIC1-76 output is normal?
No
Check RIC1-36 terminal.
Yes
Yes
Pick-up transfer smooth.
No
Check MECHA.
Yes
SIC4-28, 29 terminal outputs are normal?
No
Check SIC4 peripheral circuit.
Yes
Check SIC1 peripheral circuit.
Check DCN1 and pick-up.

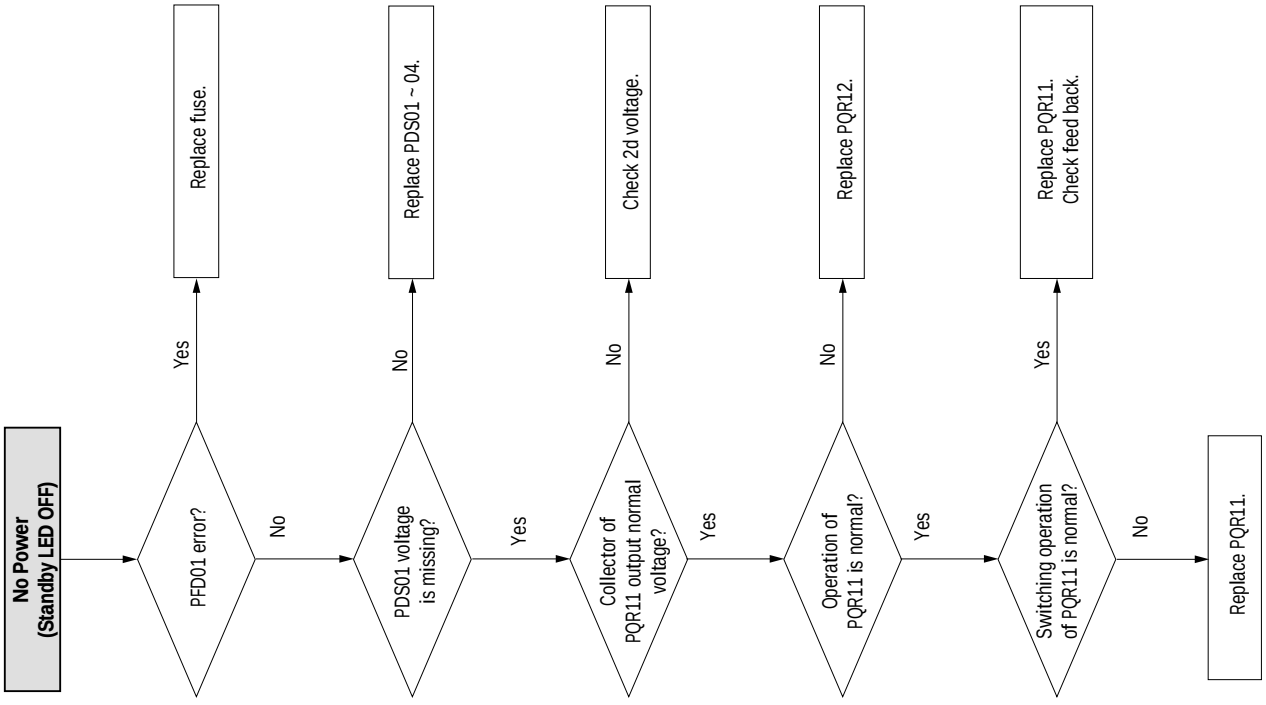

No Tray open/close
MIC1-84, 85 is
Open : "L", "L" ?
Close : "H", "H"?
No
Micom (MIC1) error.
Yes
Check SIC4-35, 36
output at open/close
No
Check SIC4.
Yes
Check signal line state from
SIC4-35, 36 to tray motor.

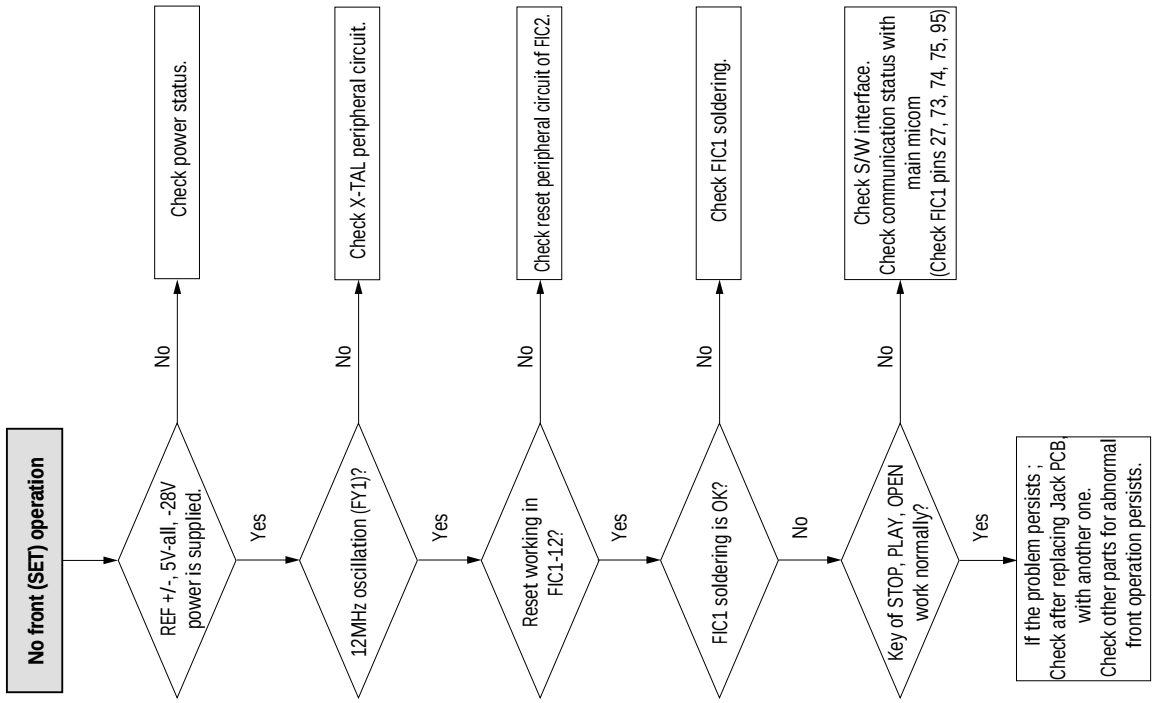

Abnormal rotation of
disc motor
Input of RF signal
is normal? (SIC1-59)
No
Check RIC1 peripheral
circuit and A, B, C, D.
Yes
RIC1-88 output
is normal?
No
Check RIC1 soldering and power.
Yes
RIC1-86 output
are normal?
No
After resoldering SIC1.
Yes
SPD output is normal?
(SIC1-74)
No
Check path to RIC1 and SIC1.
Yes
Check DRIC1 soldering and power.
SIC4-2 output (FG)
is normal?
No
Check DIC1, MIC1.
Yes
SIC4-9 signal
MON is "H" ?
No
Check or replace disc motor.
Yes

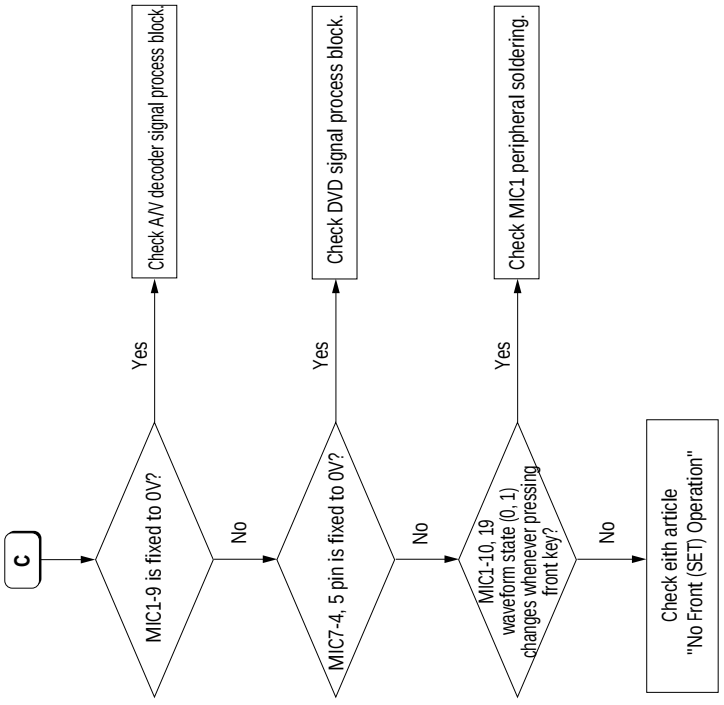

Digital output error
Output in ZIC1-127 is normal?
No
Check ZIC1 peripheral circuit.
Yes
Output in AIC3-6, 8, 10 is normal?
No
Check AIC3.
Yes
Check AVJ4, 5 peripheral soldering shot.

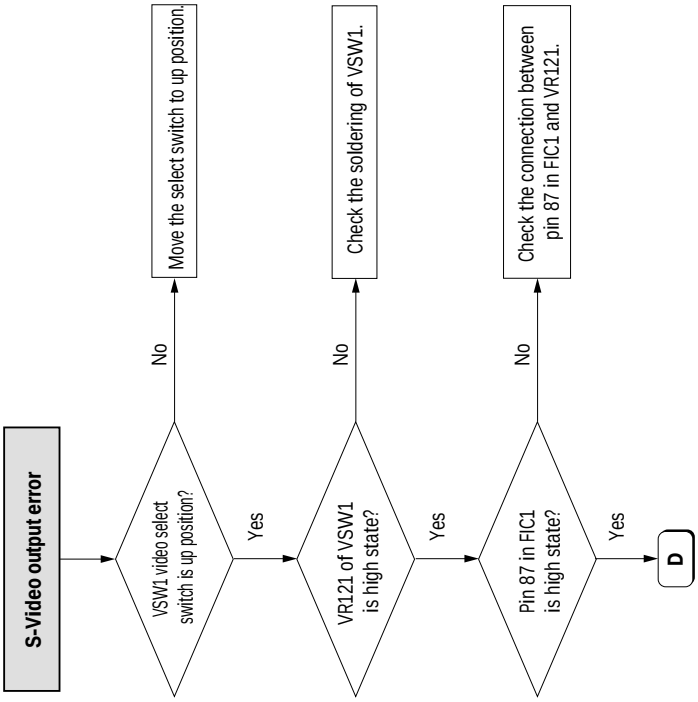

CD/VCD/DVD L/R output error (Mixed Audio output)
Normal DATA 0 is input in AIC1-6?
No
Check ZIC1-121 output.
Yes
Analog output of AIC1-20, 21, 22, 23 is normal?
No
Check ZIC1-125 (CD/VCD ; 16.9344MHz, DVD ; 18.432MHz)
Yes
AOP1-1, 7 output is normal?
No
Check AOP1 peripheral circuit.
Yes
Base terminal level of AQ1, AQ3 are "L"?
No
Check FIC1-47 mute.
Yes
Check AVJ2 peripheral soldering shot.

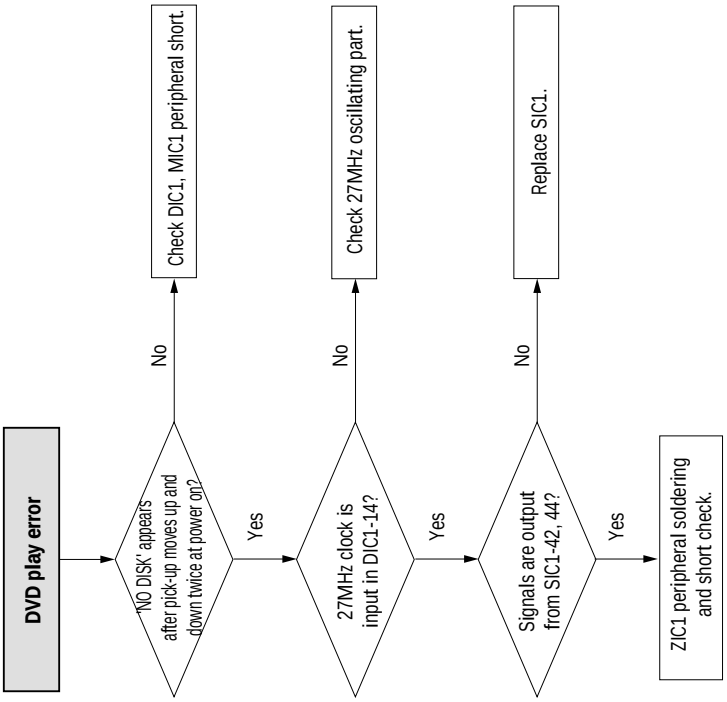

Key operation or remote control error
All power is measured correctly and front cable is properly connected?
Yes
Check A/V decoder signal process block.
Yes
All clocks (20MHz, 33.8688MHz, 27MHz) of main PCB oscillate normally?
No
Check all clock oscillating parts.
Yes
/CS2, /RD, /WR signal occur?
No
Check short pin out of micom common-bus (8-bit).
Check short or operating of micom.
Check soldering of micom and communication devices.
Yes
Play works?
No
Check ZIC1 peripheral unit.
Yes
C

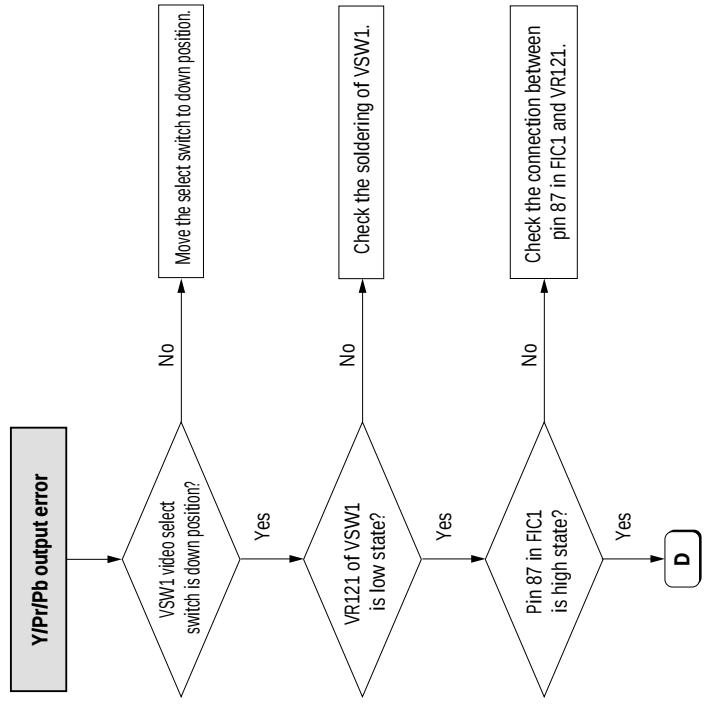

No Power (Standby LED OFF)
PFD01 error?
Yes
Replace fuse.
No
PDS01 voltage is missing?
No
Replace PDS01 ~ 04.
Yes
Collector of PQR11 output normal voltage?
No
Check 2d voltage.
Yes
Operation of PQR11 is normal?
No
Replace PQR12.
Yes
Switching operation of PQR11 is normal?
Yes
Replace PQR11. Check feed back.
No
Replace PQR11.

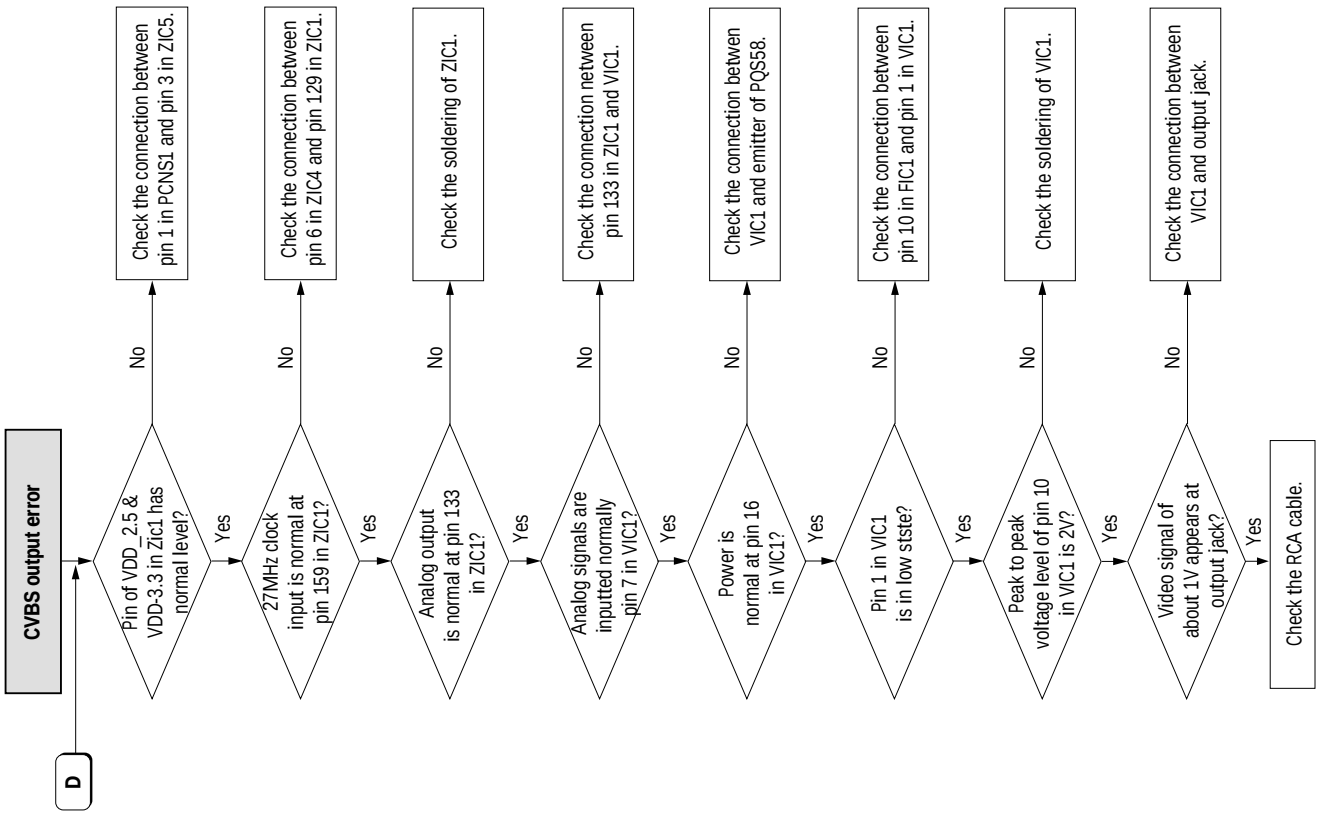

No front (SET) operation
REF +/-, 5V-all, -28V power is supplied.
No
Check power status.
Yes
12MHz oscillation (FY1)?
No
Check X-TAL peripheral circuit.
Yes
Reset working in FIC1-12?
No
Check reset peripheral circuit of FIC2.
Yes
FIC1 soldering is OK?
No
Check FIC1 soldering.
No
Key of STOP, PLAY, OPEN work normally?
No
Check S/W interface.
Check communication status with main micom
(Check FIC1 pins 27, 73, 74, 75, 95)
Yes
If the problem persists ;
Check after replacing Jack PCB with another one.
Check other parts for abnormal front operation persists.


C
MIC1-9 is fixed to 0V?
Yes
Check A/V decoder signal process block.
No
MIC7-4, 5 pin is fixed to 0V?
Yes
Check DVD signal process block.
No
MIC1-10, 19 waveform state (0, 1) changes whenever pressing front key?
Yes
Check MIC1 peripheral soldering.
No
Check eith article
"No Front (SET) Operation"


S-Video output error
VSW1 video select switch is up position?
No
Move the select switch to up position.
Yes
VR121 of VSW1 is high state?
No
Check the soldering of VSW1.
Yes
Pin 87 in FIC1 is high state?
No
Check the connection between pin 87 in FIC1 and VR121.
Yes
D


DVD play error
'NO DISK' appears after pick-up moves up and down twice at power on?
No
Check DIC1, MIC1 peripheral short.
Yes
27MHz clock is input in DIC1-14?
No
Check 27MHz oscillating part.
Yes
Signals are output from SIC1-42, 44?
No
Replace SIC1.
Yes
ZIC1 peripheral soldering and short check.


Y/Pr/Pb output error
VSW1 video select switch is down position?
No
Move the select switch to down position.
Yes
VR121 of VSW1 is low state?
No
Check the soldering of VSW1.
Yes
Pin 87 in FIC1 is high state?
No
Check the connection between pin 87 in FIC1 and VR121.
Yes
D

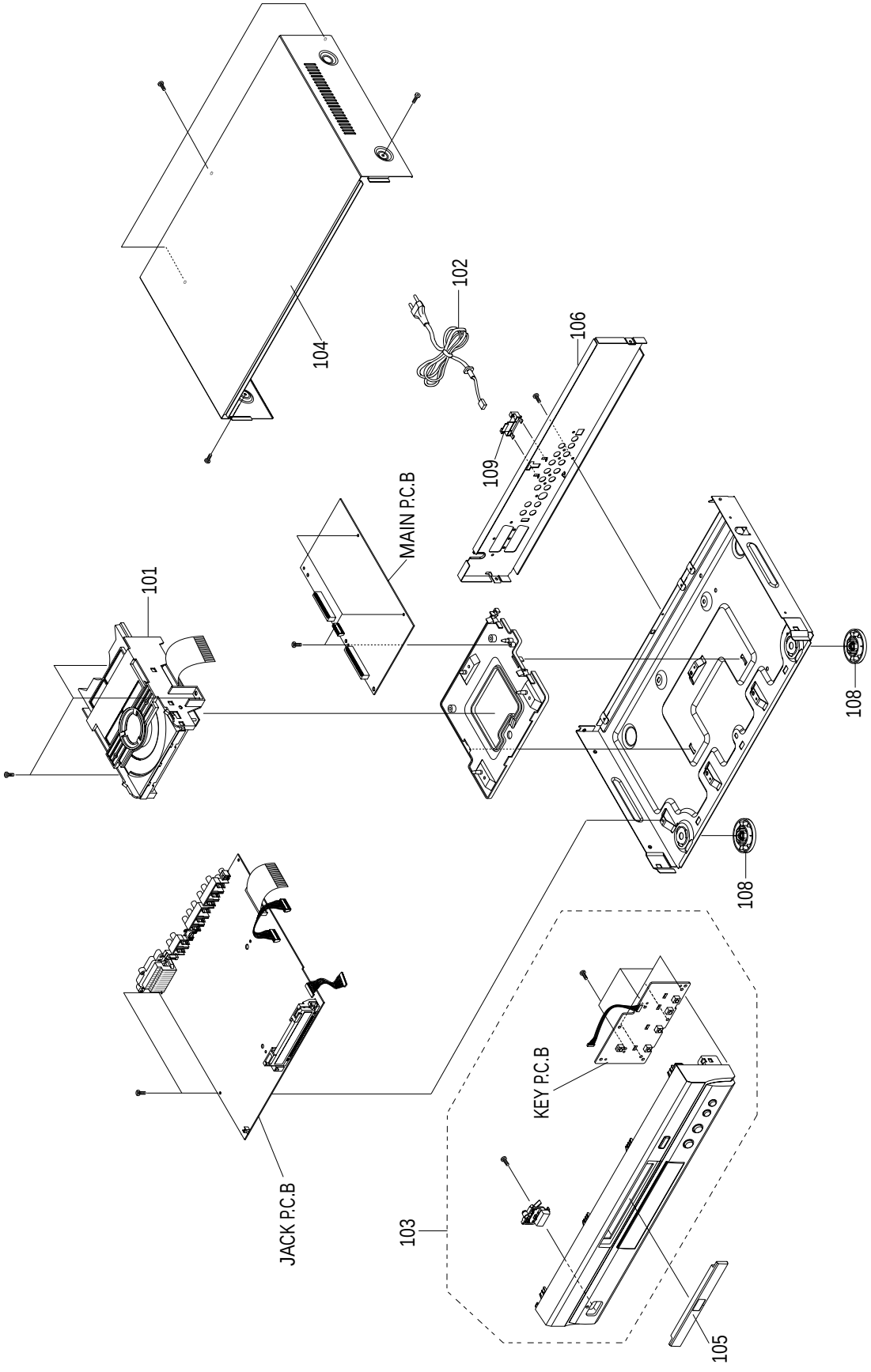

CVBS output error
D
Pin of VDD_2.5 & VDD-3.3 in Zic1 has normal level?
No
Check the connection between pin 1 in PCNS1 and pin 3 in ZIC5.
Yes
27MHz clock input is normal at pin 159 in ZIC1?
No
Check the connection between pin 6 in ZIC4 and pin 129 in ZIC1.
Yes
Analog output is normal at pin 133 in ZIC1?
No
Check the soldering of ZIC1.
Yes
Analog signals are inputted normally pin 7 in VIC1?
No
Check the connection netween pin 133 in ZIC1 and VIC1.
Yes
Power is normal at pin 16 in VIC1?
No
Check the connection betwn VIC1 and emitter of PQS58.
Yes
Pin 1 in VIC1 is in low stste?
No
Check the connection between pin 10 in FIC1 and pin 1 in VIC1.
Yes
Peak to peak voltage level of pin 10 in VIC1 is 2V?
No
Check the soldering of VIC1.
Yes
Video signal of about 1V appears at output jack?
No
Check the connection between VIC1 and output jack.
Yes
Check the RCA cable.

MEMO

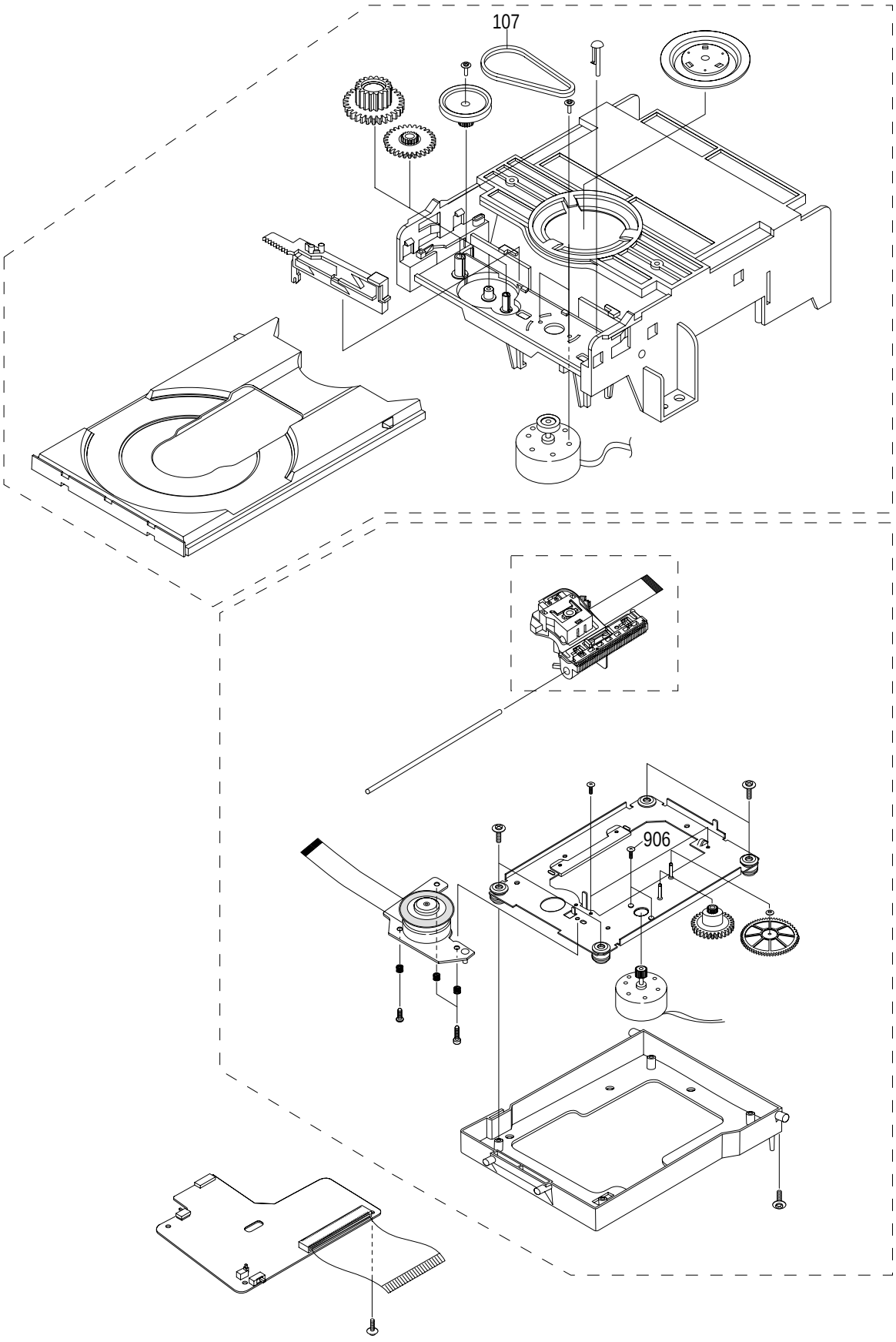
8. Exploded View

	Page
8-1 Cabinet Assembly	8-2
8-2 Deck Assembly	8-3

8-1 Cabinet Assembly



8-2 Deck Assembly



MEMO

9. Replacement Parts List

1. MECHANICAL PARTS LIST

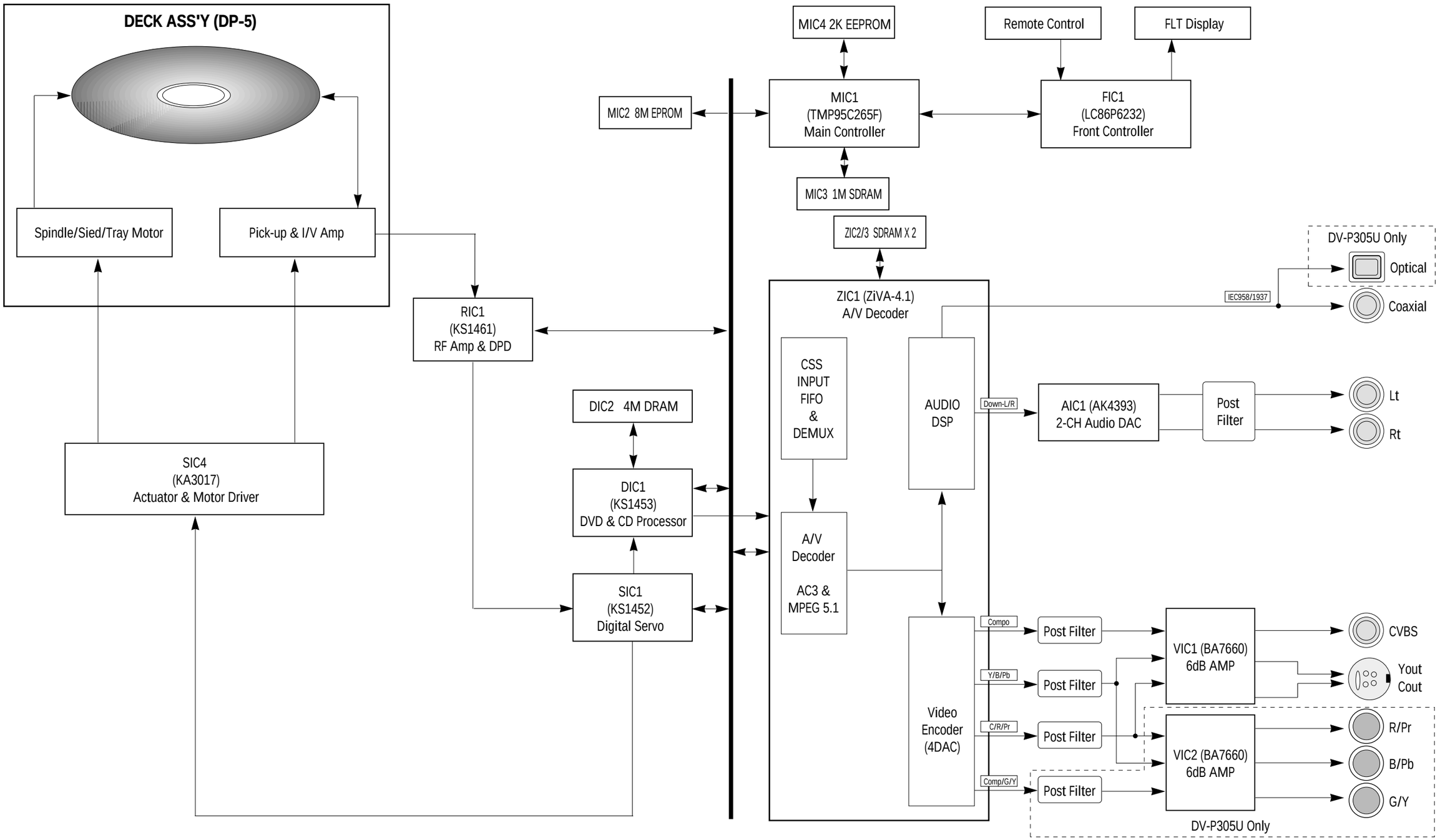
SYMBOL NO	P-NO	DESCRIPTION	
		MECHINISM SECTION	
101	TS15531	MECHA ASSY(DVD)	
102	TE13371	CORD,POWER	
103	TJ14101	PANEL,FRONT	[DV-P303U]
103	TJ14102	PANEL,FRONT	[DV-P305U]
104	TJ14121	COVER,TOP	
105	TJ14141	DOOR ASSY	
106	TJ14162	PANEL,REAR	
107	TJ14211	BELT	
108	TJ14241	FOOT, FRONT	
109	TJ14251	HOLDER,CORD	
		ACCESSORIES	
802	TS15541	REMOTE HAND SET	
803	TE13361	CORD,AV	

2. ELECTRICAL PARTS LIST

SYMBOL NO	P-NO	DESCRIPTION
MIC2	TC11291	IEPROM(P303U)
CN8	TE13381	CONNECTOR
DCN1	TE13391	CONNECTOR
PFD01	TE13401	FUSE

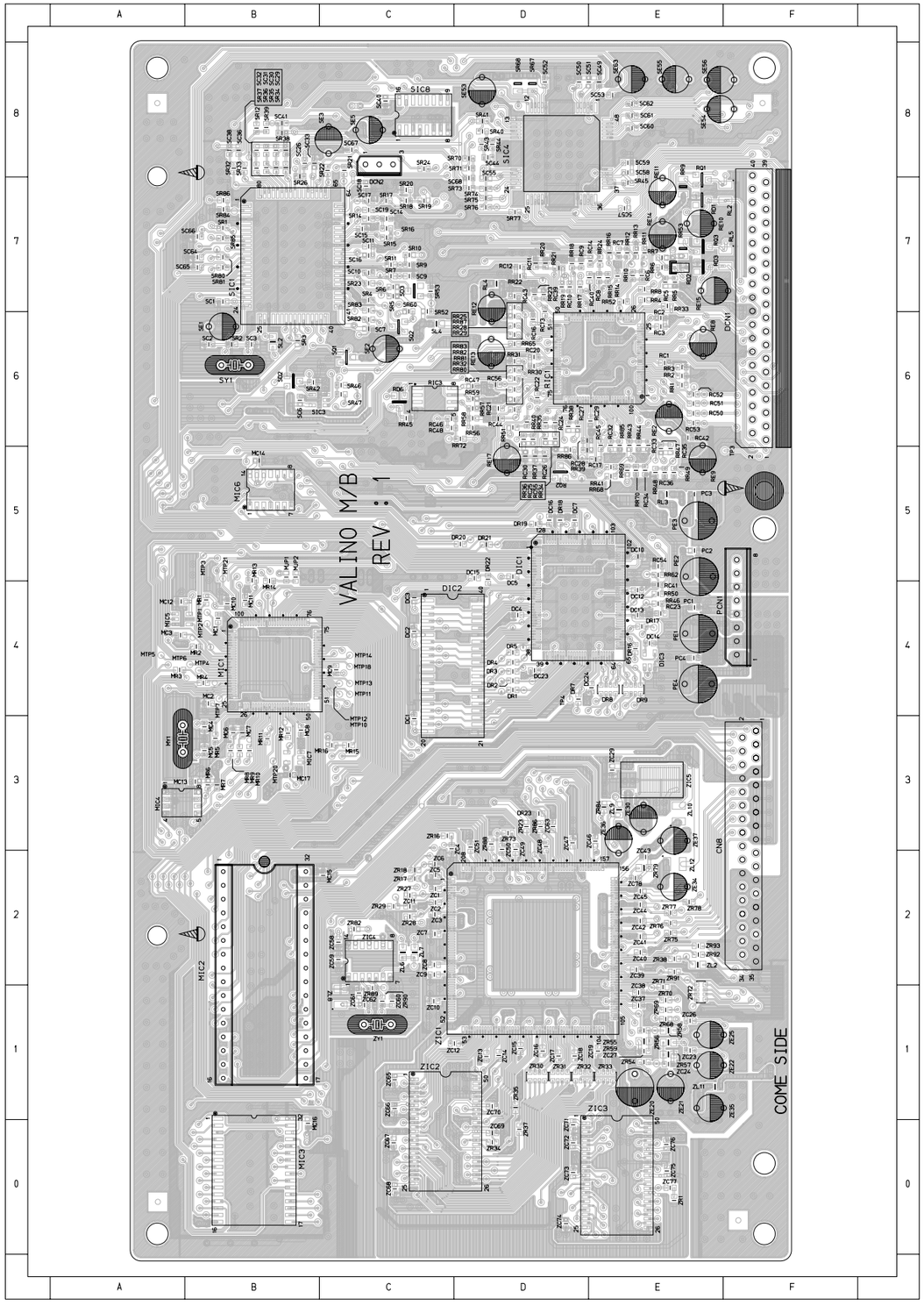
MEMO

10. Block Diagram

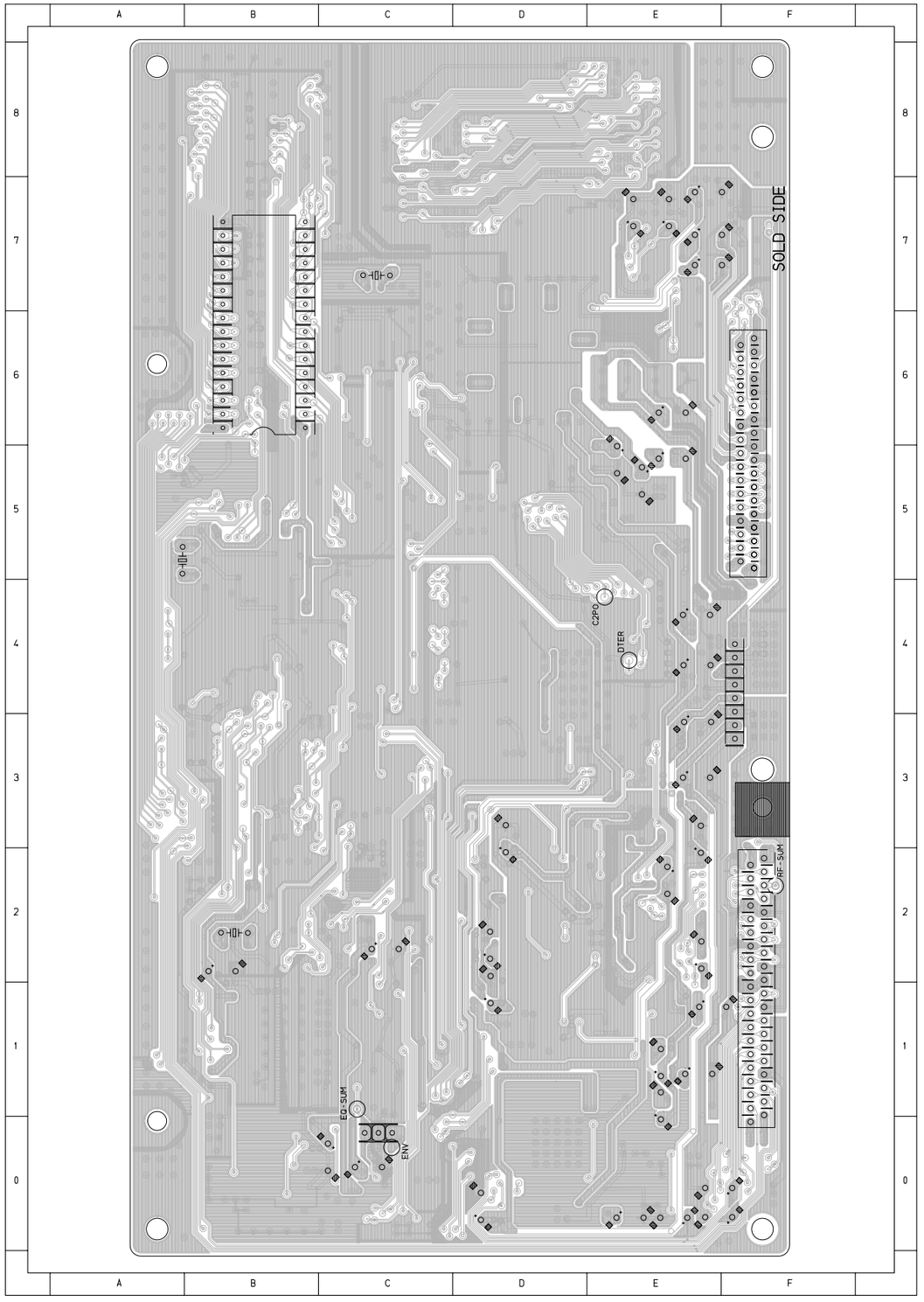


11-1 Main

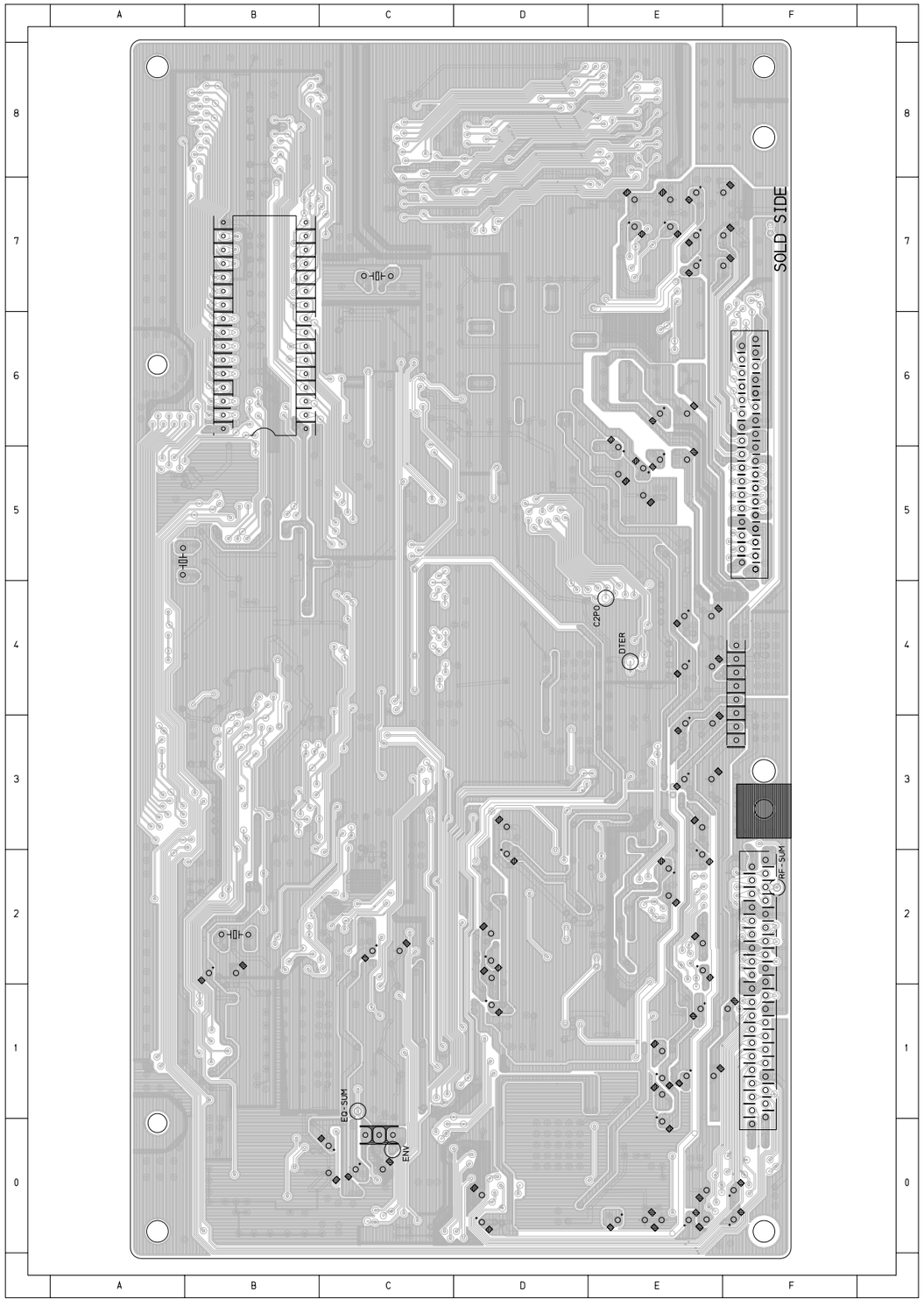
COMPONENT



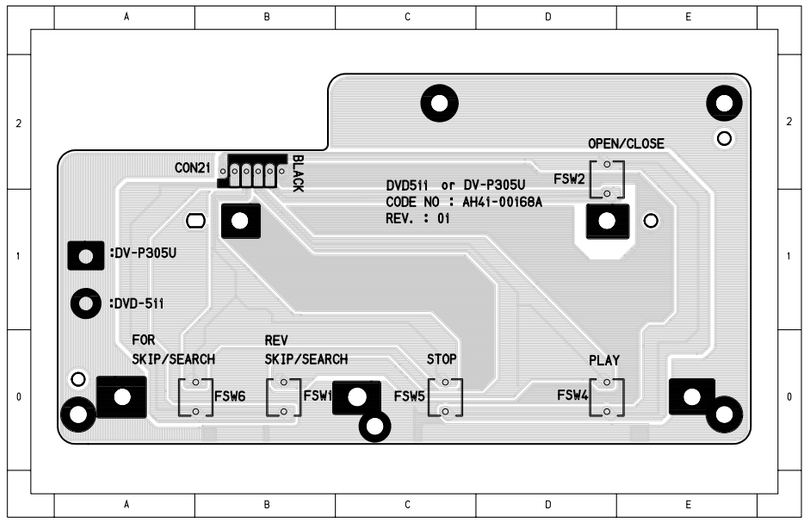
SOLDER SIDE



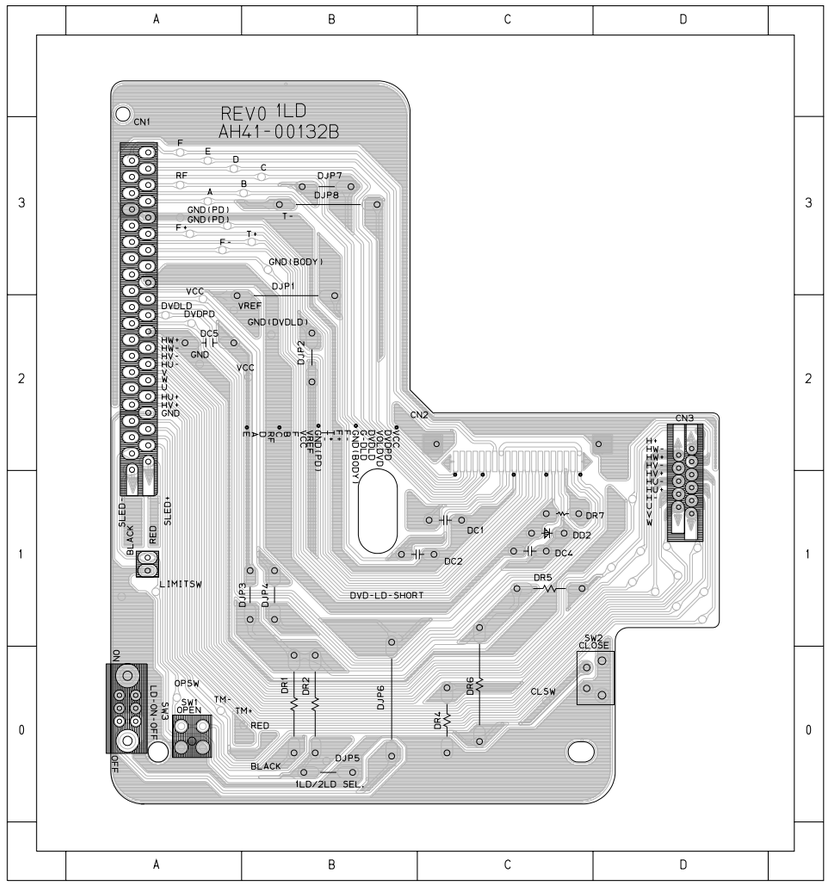
11-2 Jack



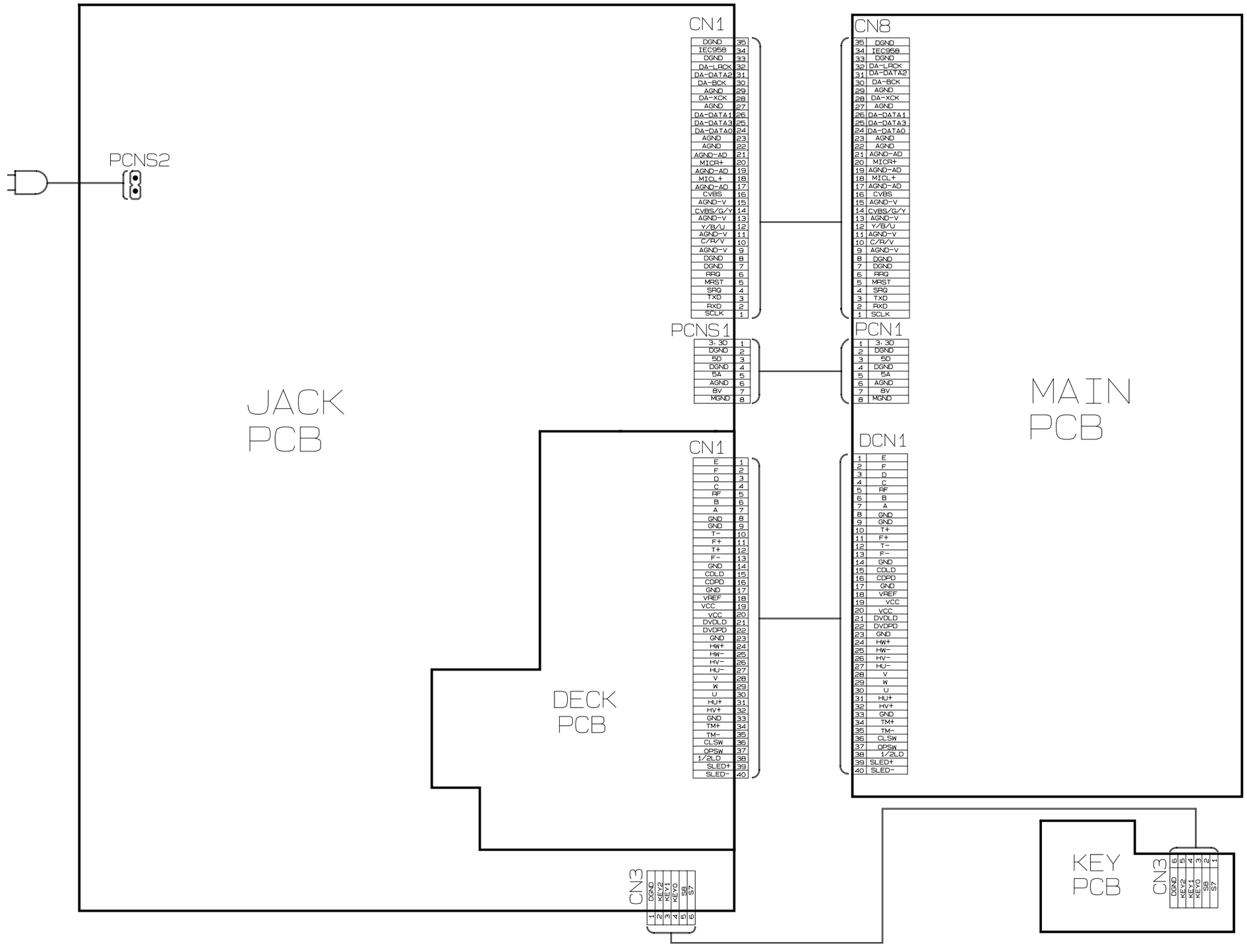
11-3 Key



11-4 Deck



12. Wiring Diagram



MEMO

13. Schematic Diagrams

13-1 Power ---------- 13-2

13-2 Main-Micom ---------- 13-3

13-3 Servo ---------- 13-4

13-4 Video ---------- 13-5

13-5 Audio ---------- 13-6

13-6 RF ---------- 13-7

13-7 ZiVA ---------- 13-8

13-8 DSP ---------- 13-9

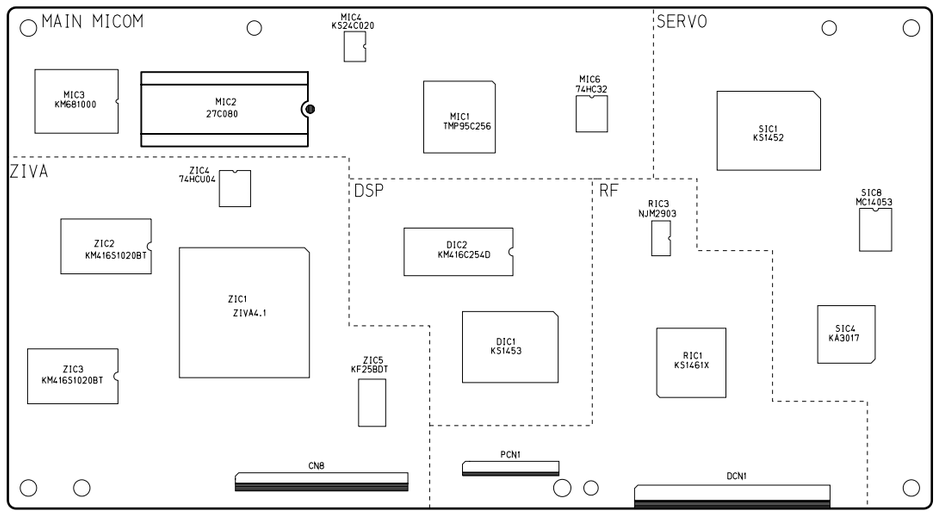
13-9 Front-Micom/VFD Display ---------- 13-10

13-10 Key ---------- 13-11

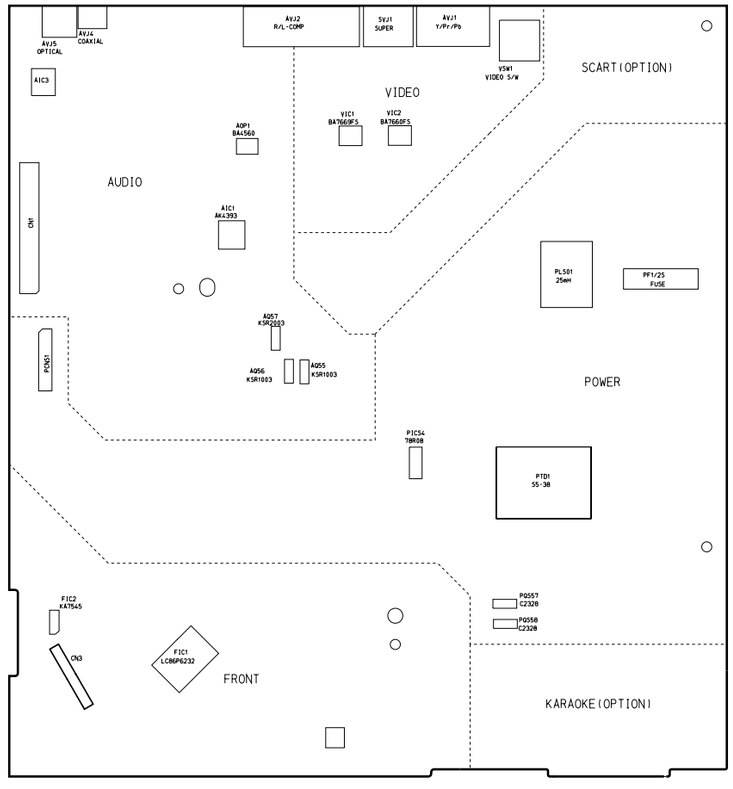
13-11 Deck ---------- 13-12

13-12 Remote Control ---------- 13-13

Block Identification of PCB

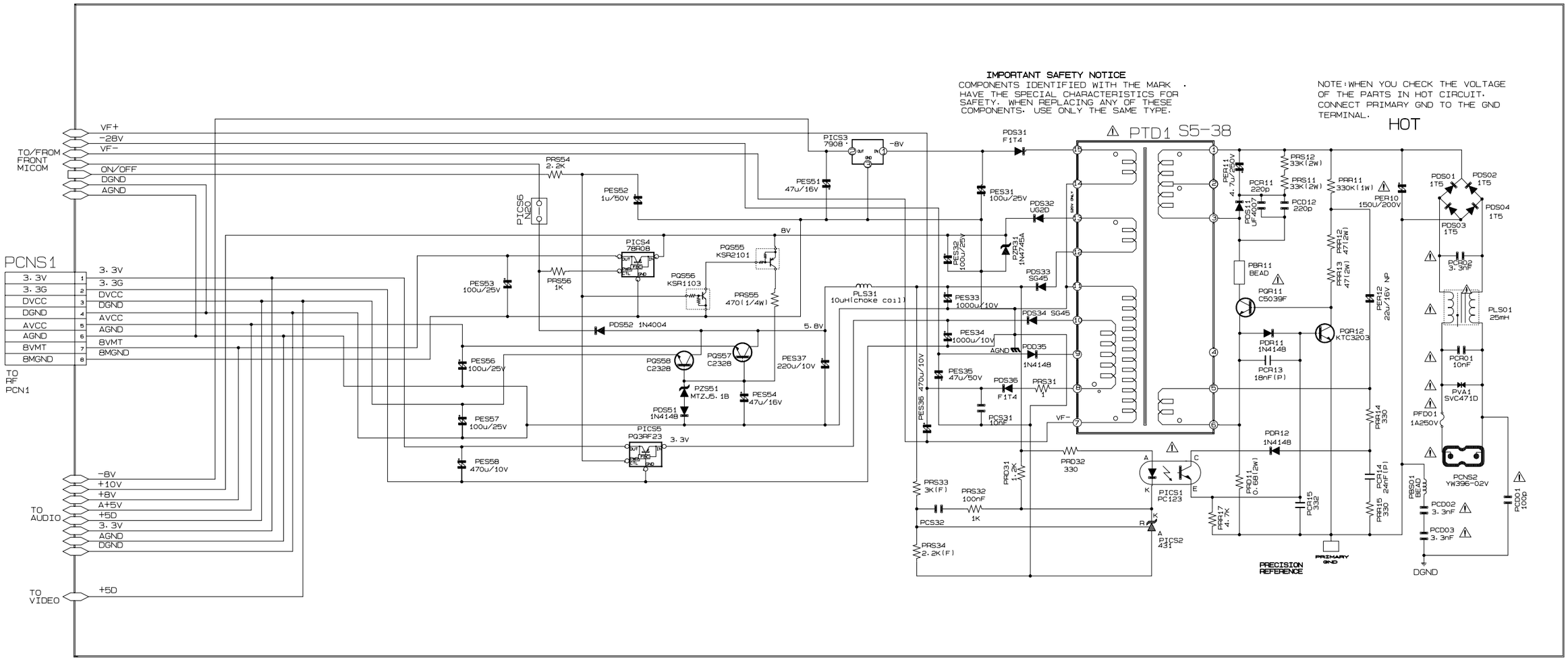


Main PCB (Component Side)

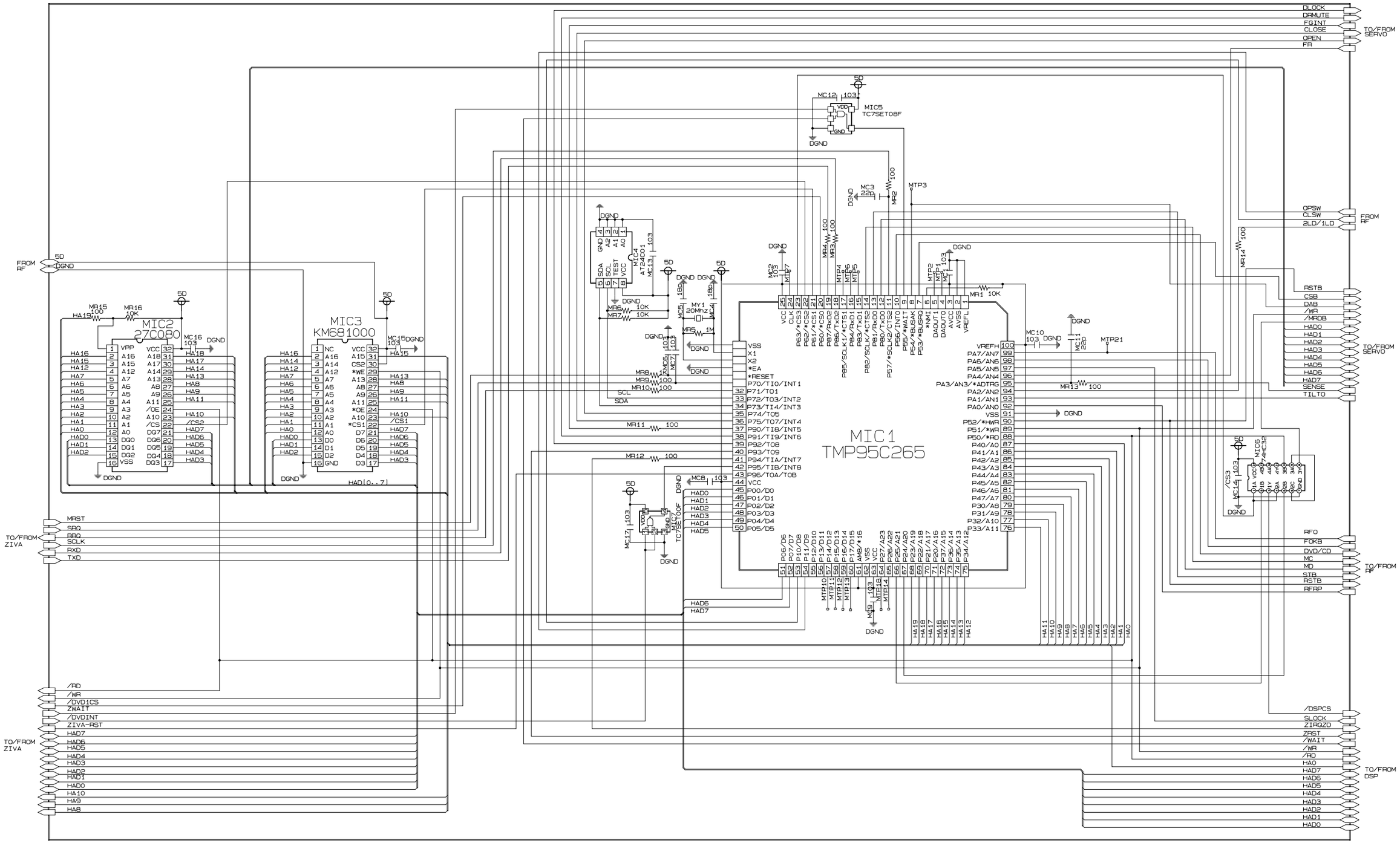


Jack PCB (Conductor Side)

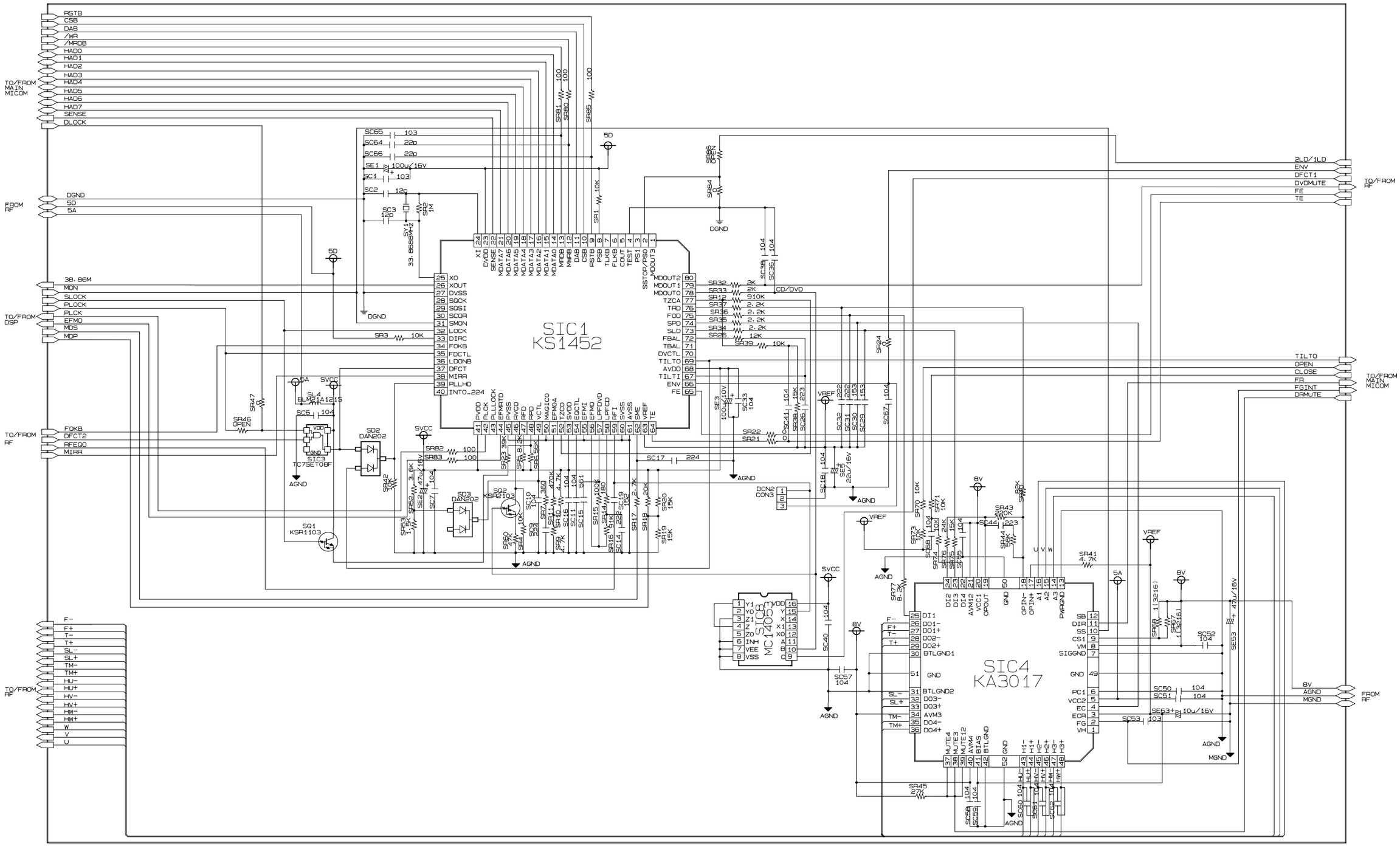
13-1 Power


IMPORTANT SAFETY NOTICE
COMPONENTS IDENTIFIED WITH THE MARK ⚠ HAVE THE SPECIAL CHARACTERISTICS FOR SAFETY. WHEN REPLACING ANY OF THESE COMPONENTS. USE ONLY THE SAME TYPE.
NOTE:WHEN YOU CHECK THE VOLTAGE OF THE PARTS IN HOT CIRCUIT. CONNECT PRIMARY GND TO THE GND TERMINAL.
HOT
⚠ PTD1 S5-38
PCNS1
TO/FROM FRONT MICOM
VF+
-28V
VF-
ON/OFF
DGND
AGND
3.3V
3.3G
DVCC
DGND
AVCC
AGND
8VMT
8MGND
TO AF PCN1
TO AUDIO
-8V
+10V
+8V
A+5V
+5D
3.3V
AGND
DGND
TO VIDEO
+5D
PICS3 7908
-8V
PRS54 2.2K
PES52 1u/50V
PES51 47u/16V
PICS6 NC
PICS4 78R08
PQS55 KSR2101
PQS56 KSR1103
PES53 100u/25V
PRS56 1K
PRS55 470(1/4W)
8V
PDS52 1N4004
5.8V
PLS31 10uH(choke coil)
PES56 100u/25V
PQS58 C2328
PQS57 C2328
PES37 220u/10V
PZS51 MTZJ5.1B
PES54 47u/16V
PDS51 1N4148
PES57 100u/25V
PICS5 PQ3RF23
3.3V
PES58 470u/10V
PDS31 F1T4
PES31 100u/25V
PDS32 UG2D
PES32 100u/25V
PZR31 1N4745A
PDS33 SG45
PES33 1000u/10V
PDS34 SG45
PES34 1000u/10V
AGND
PDD35 1N4148
PES35 47u/50V
PDS36 F1T4
PRS31 1
PES36 470u/10V
PCS31 10nF
VF-
PRD31 1.2K
PRD32 330
PRS33 3K(F)
PRS32 100nF
1K
PCS32
PRS34 2.2K(F)
PICS1 PC123
PICS2 431
PRECISION REFERENCE
PRIMARY GND
PER11 4.7U/250V
PCR11 220p
PFD01 UF2017
PRS12 33K(2W)
PRS11 33K(2W)
PRR11 330K(1W)
PER10 150U/200V
PCD12 220p
PBR11 BEAD
PQR11 C5039F
PRR12 47(2W)
PRR13 47(2W)
PQR12 KTC3203
PDR11 1N4148
PCR13 18nF(P)
PDR12 1N4148
PRD11 0.68(2W)
PRR17 4.7K
PCR15 332
PER12 22U/16V NP
PRR14 330
PCR14 24nF(P)
PRR15 330
PDS01 1T5
PDS02 1T5
PDS04 1T5
PDS03 1T5
PCR02 3.3nF
PLS01 25mH
PCR01 10nF
PVA1 SVC471D
PFD01 1A250V
PCNS2 YW396-02V
PBS01 BEAD
PCD02 3.3nF
PCD03 3.3nF
PCD01 100p
DGND

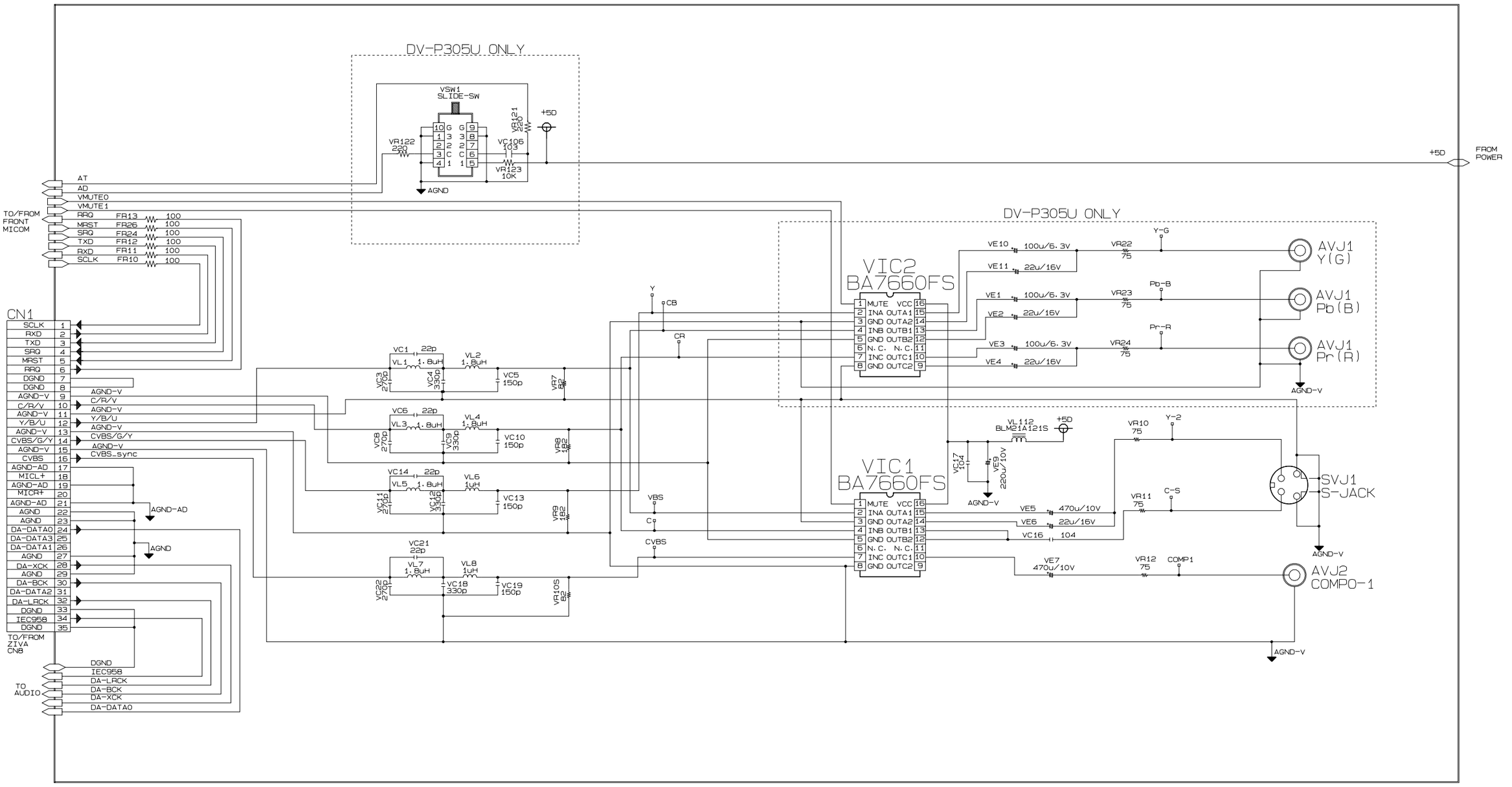
13-2 Main-Micom



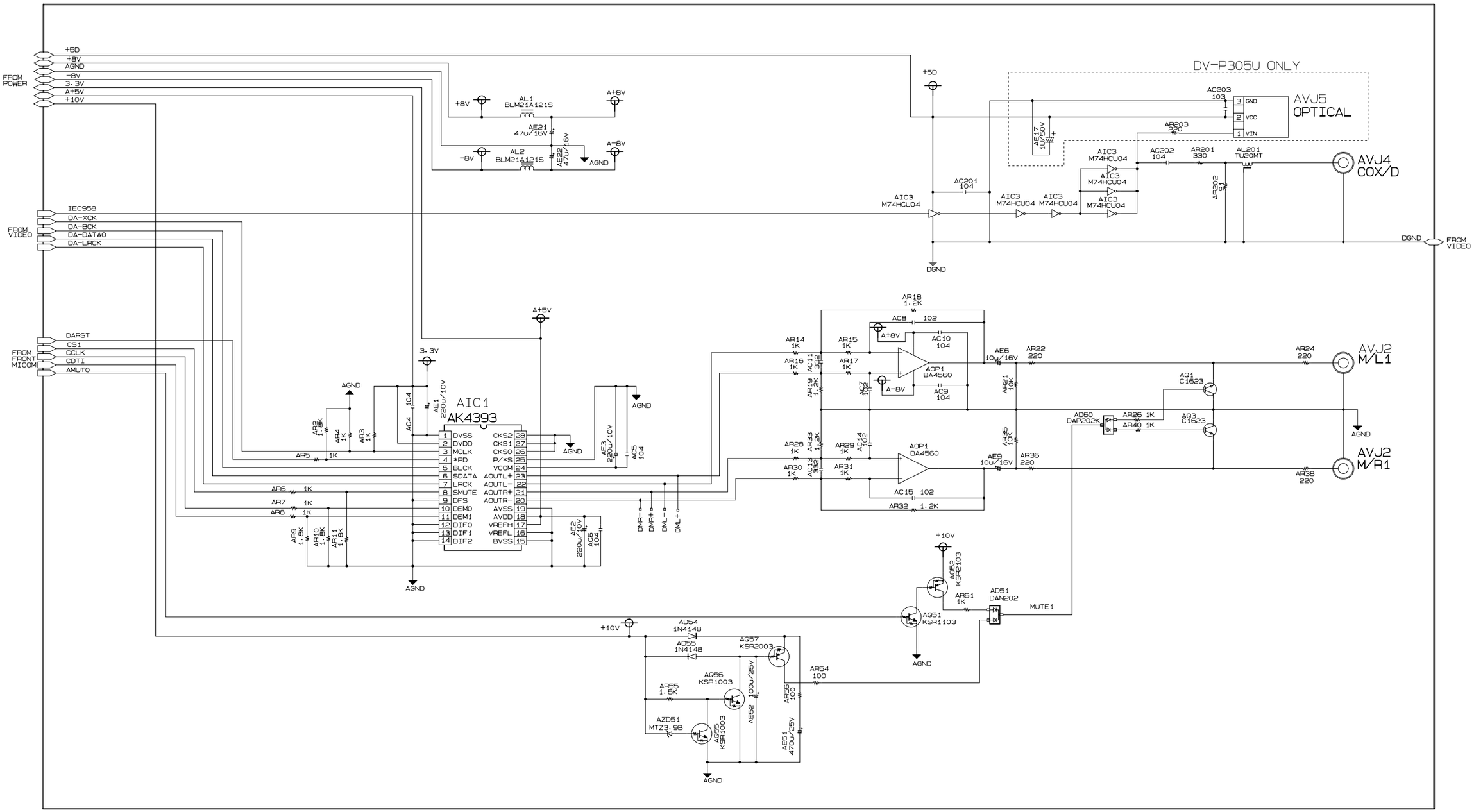
13-3 Servo


SIC1
KS1452
SIC3
TC7SET08F
SIC4
KA3017
SIC5
MC14053
SQ1
KSR1103
SQ2
KSR2103
SD2
DAN202
SD3
DAN202
TO/FROM MAIN MICOM
FROM RF
TO/FROM DSP
TO/FROM RF
TO/FROM MAIN MICOM
FROM RF
RSTB
CSB
DAB
/WR
/MRDB
HAD0
HAD1
HAD2
HAD3
HAD4
HAD5
HAD6
HAD7
SENSE
DLOCK
DGND
5D
5A
38.86M
MON
SLOCK
PLOCK
PLCK
EFMO
MDS
MDP
FOKB
DFCT2
RFEQO
MIRR
F-
F+
T-
T+
SL-
SL+
TM-
TM+
HU-
HU+
HV-
HV+
HW-
HW+
W
V
U
SVCC
AGND
VREF
8V
2LD/1LD
ENV
DFCT1
DVDMUTE
FE
TE
CD/DVD
TILTO
OPEN
CLOSE
FR
FGINT
DRMUTE
8V
AGND
MGND

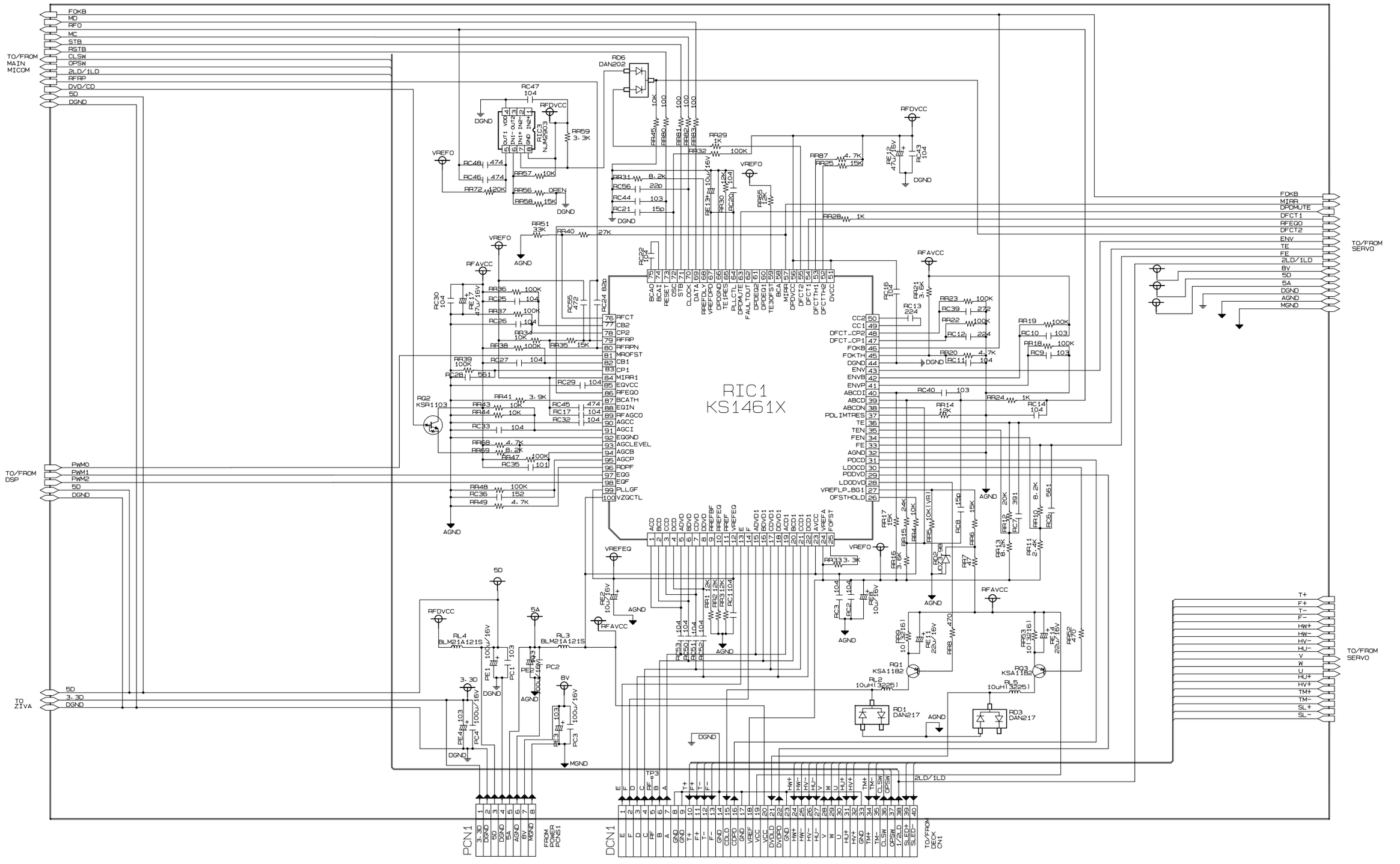
13-4 Video


DV-P305U ONLY
VSW1
SLIDE-SW
VR122
220
VR121
220
VC106
103
VR123
10K
+5D
AGND
FROM
POWER
AT
AD
VMUTE0
VMUTE1
TO/FROM
FRONT
MICOM
ARQ FR13 100
MRST FR26 100
SRQ FR24 100
TXD FR12 100
RXD FR11 100
SCLK FR10 100
CN1
SCLK 1
RXD 2
TXD 3
SRQ 4
MRST 5
ARQ 6
DGND 7
DGND 8
AGND-V 9
C/B/V 10
AGND-V 11
Y/B/U 12
AGND-V 13
CVBS/G/Y 14
AGND-V 15
CVBS 16
AGND-AD 17
MICL+ 18
AGND-AD 19
MICR+ 20
AGND-AD 21
AGND 22
AGND 23
DA-DATA0 24
DA-DATA3 25
DA-DATA1 26
AGND 27
DA-XCK 28
AGND 29
DA-BCK 30
DA-DATA2 31
DA-LRCK 32
DGND 33
IEC958 34
DGND 35
TO/FROM
ZIVA
CN8
DGND
IEC958
DA-LRCK
DA-BCK
DA-XCK
DA-DATA0
TO
AUDIO
AGND-AD
AGND
AGND-V
C/B/V
AGND-V
Y/B/U
AGND-V
CVBS/G/Y
AGND-V
CVBS_sync
VC1 22p
VL1 1.8uH
VL2 1.8uH
VC3 270p
VC4 330p
VC5 150p
VR7 82
VC6 22p
VL3 1.8uH
VL4 1.8uH
VC8 270p
VC9 330p
VC10 150p
VR8 82
VC14 22p
VL5 1.8uH
VL6 1uH
VC11 270p
VC12 330p
VC13 150p
VR9 82
VC21 22p
VL7 1.8uH
VL8 1uH
VC22 270p
VC18 330p
VC19 150p
VR10S 82
Y
CB
CR
VBS
C
CVBS
DV-P305U ONLY
VIC2
BA7660FS
MUTE VCC
INA OUTA1
GND OUTA2
INB OUTB1
GND OUTB2
N.C. N.C.
INC OUTC1
GND OUTC2
VE10 100u/6.3V
VE11 22u/16V
VE1 100u/6.3V
VE2 22u/16V
VE3 100u/6.3V
VE4 22u/16V
VR22 75
VR23 75
VR24 75
Y-G
Pb-B
Pr-R
AVJ1
Y(G)
AVJ1
Pb(B)
AVJ1
Pr(R)
AGND-V
VIC1
BA7660FS
MUTE VCC
INA OUTA1
GND OUTA2
INB OUTB1
GND OUTB2
N.C. N.C.
INC OUTC1
GND OUTC2
VL112
BLM21A121S
+5D
VC17
104
VE9
220u/10V
AGND-V
VR10
75
Y-2
VR11
75
C-S
VE5 470u/10V
VE6 22u/16V
VC16 104
VE7
470u/10V
VR12
75
COMP1
SVJ1
S-JACK
AVJ2
COMPO-1
AGND-V
AGND-V

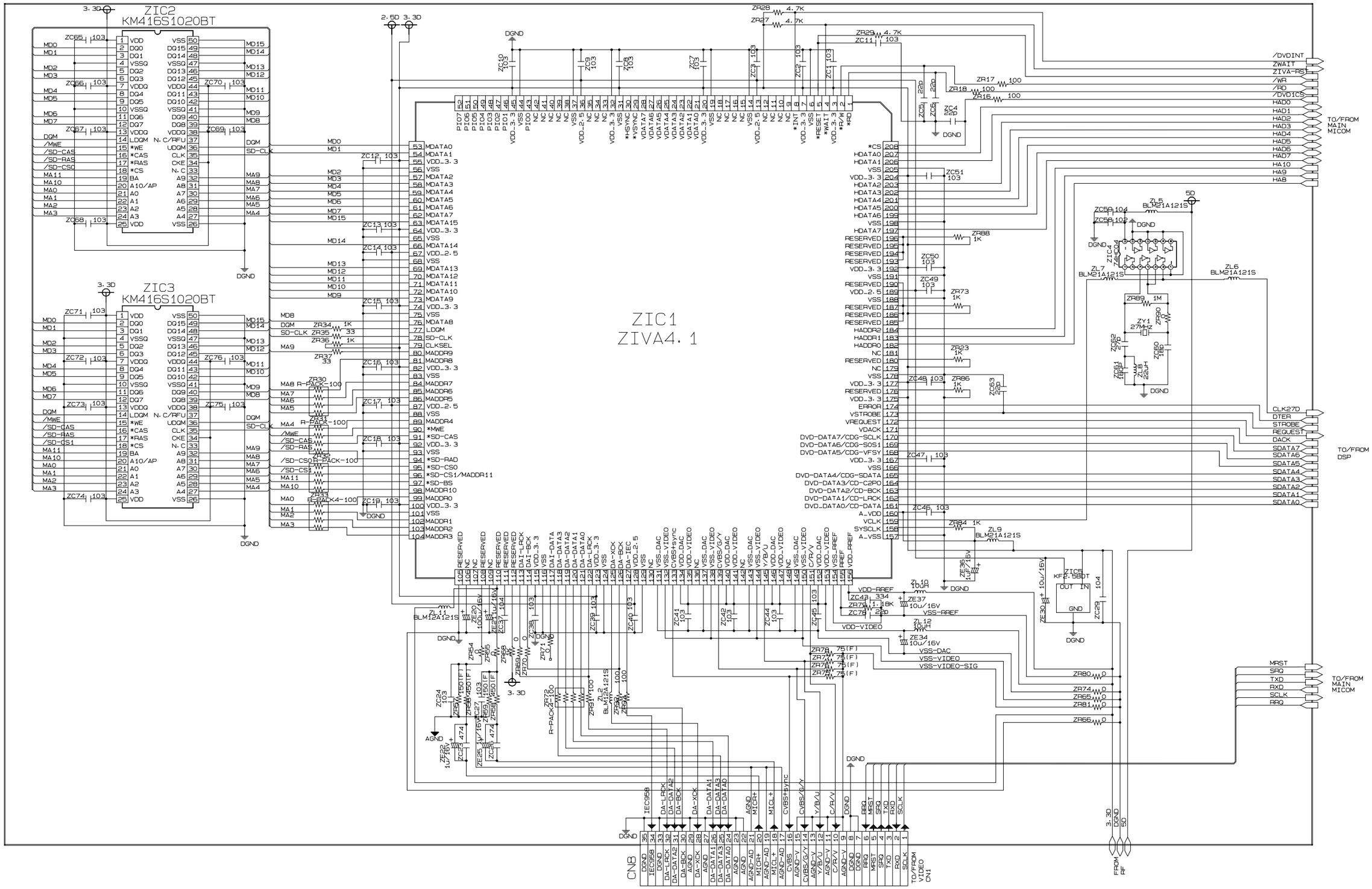
13-5 Audio


FROM POWER
+5D
+8V
AGND
-8V
3.3V
A+5V
+10V
AL1 BLM21A121S
AL2 BLM21A121S
AE21 47U/16V
AE22 47U/16V
A+8V
A-8V
DV-P305U ONLY
AVJ5 OPTICAL
AC203 103
AR203 330
AE17 1U/50V
AIC3 M74HCU04
AC202 104
AR201 330
AL201 TU20MT
AR202 0
AVJ4 COX/D
AC201 104
DGND
FROM VIDEO
IEC958
DA-XCK
DA-BCK
DA-DATA0
DA-LRCK
FROM FRONT MICOM
DARST
CS1
CCLK
CDTI
AMUTO
AIC1
AK4393
DVSS
DVDD
MCLK
*PD
BLCK
SDATA
LRCK
SMUTE
DFS
DEMO
DEM1
DIF0
DIF1
DIF2
CKS2
CKS1
CKS0
P/*S
VCOM
AOUTL+
AOUTL-
AOUTR+
AOUTR-
AVSS
AVDD
VREFH
VREFL
BVSS
AE1 220U/10V
AE2 220U/10V
AE3 220U/10V
AC4 104
AC5 104
AR2 1.8K
AR3 1K
AR4 1K
AR5 1K
AR6 1K
AR7 1K
AR8 1K
AR9 1.8K
AR10 1.8K
AR11 1.8K
DMR-
DMR+
DML-
DML+
AOP1 BA4560
AR18 1.2K
AC8 102
AC10 104
AC9 104
AR14 1K
AR15 1K
AR16 1K
AR17 1K
AC11 102
AC7 102
AR19 1K
AE6 10U/16V
AR22 220
AR21 10K
AQ1 C1623
AQ3 C1623
AD60 DAP202K
AR26 1K
AR40 1K
AR24 220
AVJ2 M/L1
AVJ2 M/R1
AR38 220
AR35 10K
AE9 10U/16V
AR36 220
AC14 102
AR28 1K
AR29 1K
AR30 1K
AR31 1K
AC15 102
AR32 1.2K
AC12 102
AR33 1.2K
AD52 KSR2103
AR51 1K
AD51 DAN202
MUTE1
AQ51 KSR1103
AD54 1N4148
AD55 1N4148
AQ57 KSR2003
AR54 100
AQ56 KSR1003
AR55 1.5K
AZD51 MTZ3.9B
AQ55 KSR1003
AE52 100U/25V
AR56 100
AE51 470U/25V

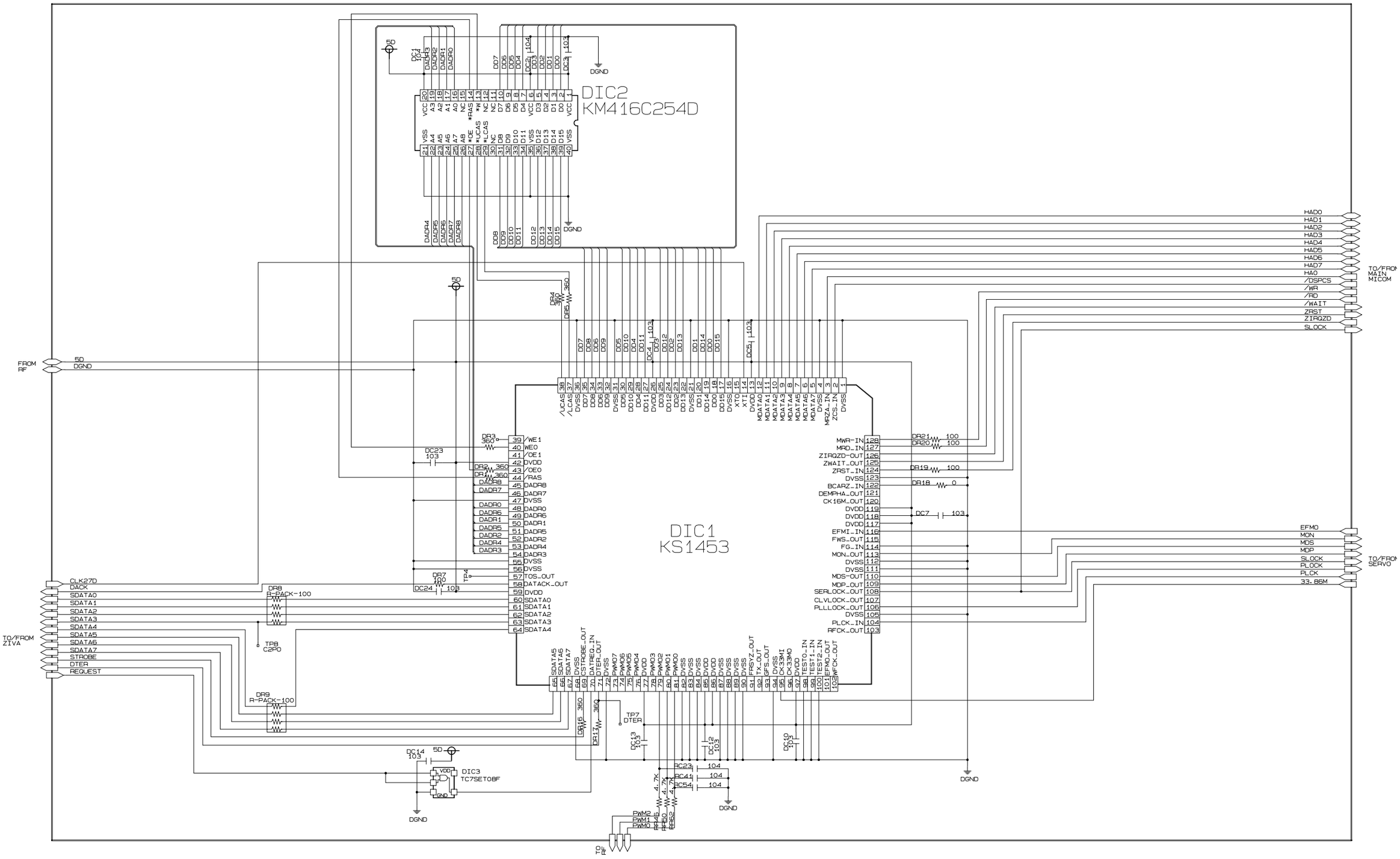
13-6 RF


RIC1
KS1461X
TO/FROM MAIN MICOM
FOKB
MD
RFO
MC
STB
RSTB
CLSW
OPSW
2LD/1LD
RFAP
DVD/CD
5D
DGND
TO/FROM DSP
PWM0
PWM1
PWM2
TO ZIVA
3.3D
TO/FROM SERVO
MIRR
DPDMUTE
DFCT1
RFEQO
DFCT2
ENV
TE
FE
8V
5A
AGND
MGND
VREFO
VREFEQ
RFAVCC
RFDVCC
DGND
PCN1
DCN1
FROM POWER PCNS1
TO/FROM DECK CN1

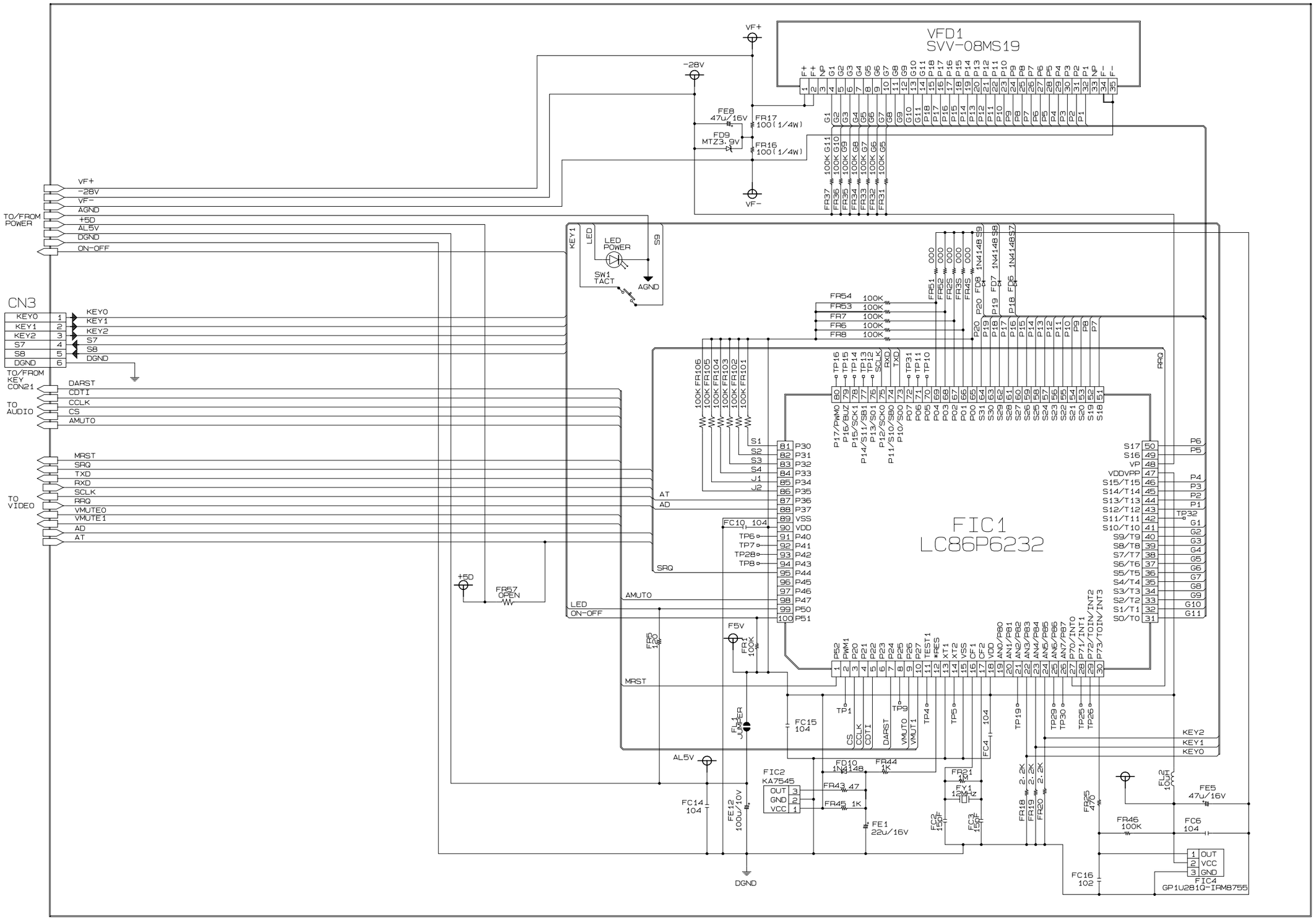
13-7 ZiVA


ZIC2
KM416S1020BT
ZIC3
KM416S1020BT
ZIC1
ZIVA4.1
CN8
TO/FROM MAIN MICOM
TO/FROM DSP
TO/FROM MAIN MICOM
TO/FROM VIDEO CN1
FROM RF

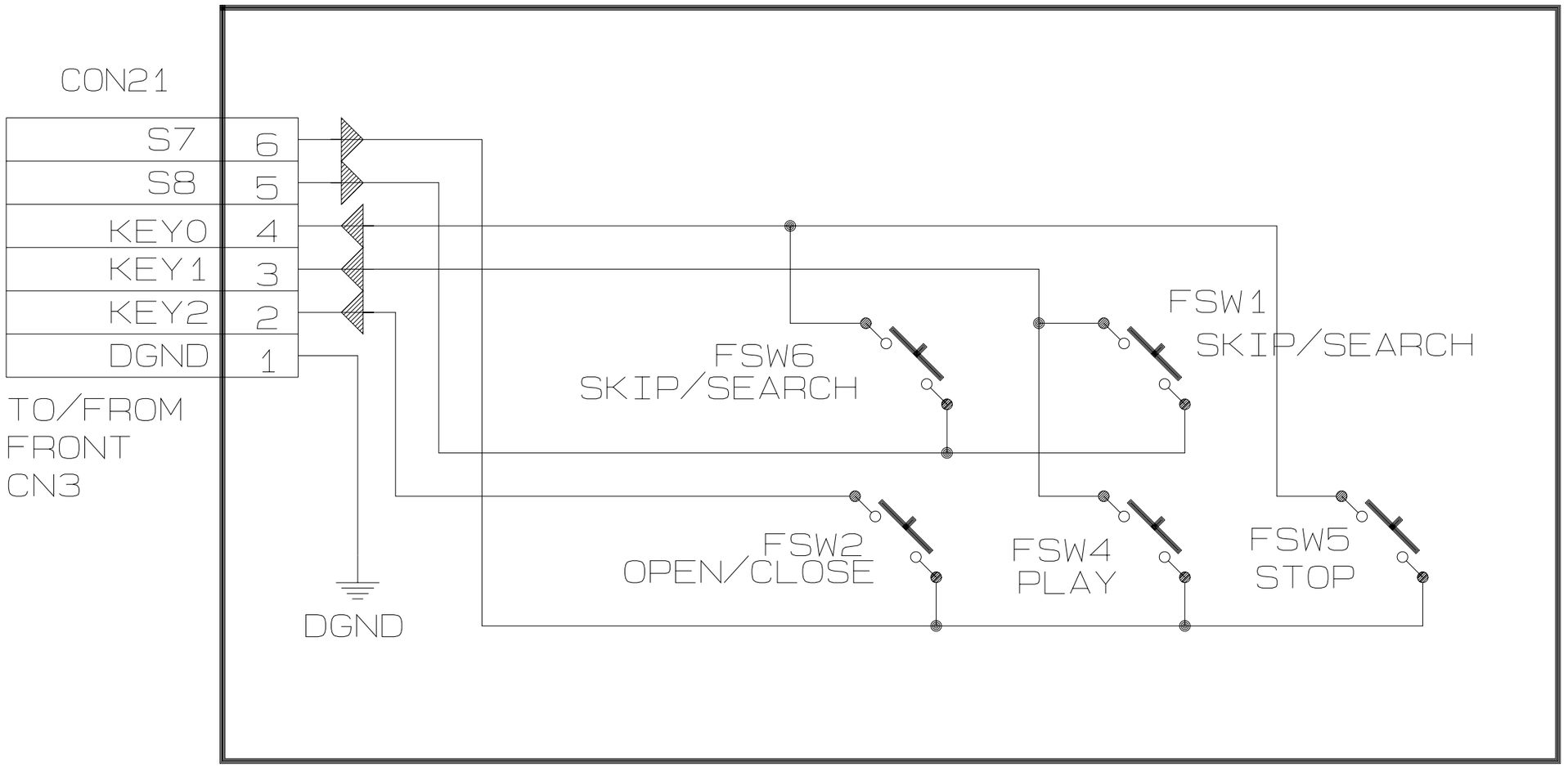
13-8 DSP


DIC2
KM416C254D
DIC1
KS1453
DIC3
TC7SET08F
5D
DGND
FROM RF
TO/FROM ZIVA
TO/FROM MAIN MICOM
TO/FROM SERVO
HAD0
HAD1
HAD2
HAD3
HAD4
HAD5
HAD6
HAD7
HA0
/DSPCS
/WR
/RD
/WAIT
ZRST
ZIRQZD
SLOCK
EFMO
MON
MDS
MDP
SLOCK
PLOCK
33.86M
CLK27D
DACK
SDATA0
SDATA1
SDATA2
SDATA3
SDATA4
SDATA5
SDATA6
SDATA7
STROBE
DTER
REQUEST
MWR-IN
MRD_IN
ZIRQZD-OUT
ZWAIT_OUT
ZRST_IN
MDP_OUT
MDS-OUT
MON_OUT
EFMI_IN
PLCK_IN
RFCK_OUT
SERLOCK_OUT
CLVLOCK_OUT
PLLLOCK_OUT
TP7 DTER
TP8 C2PO

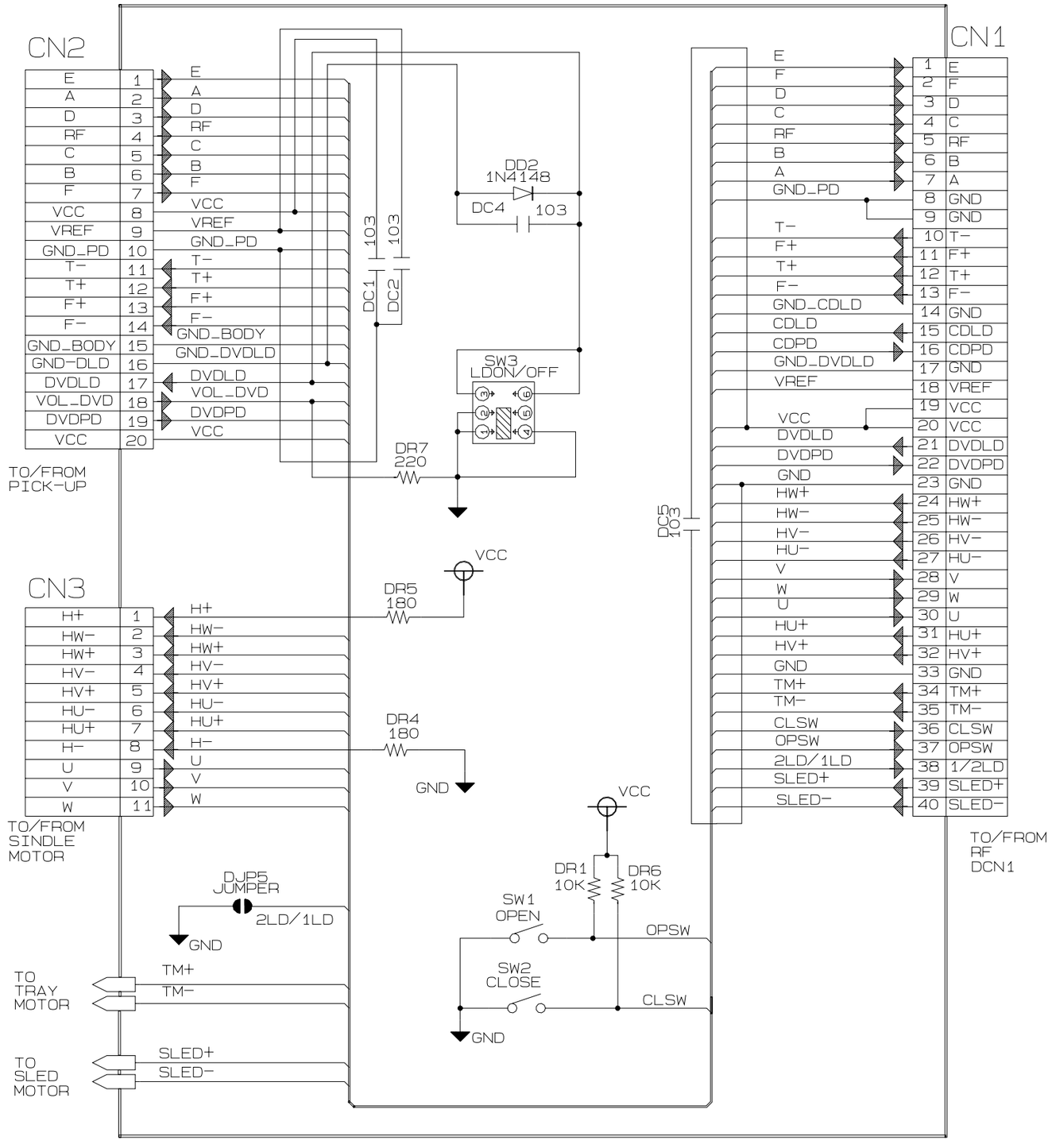
13-9 Front-Micom/VFD Display



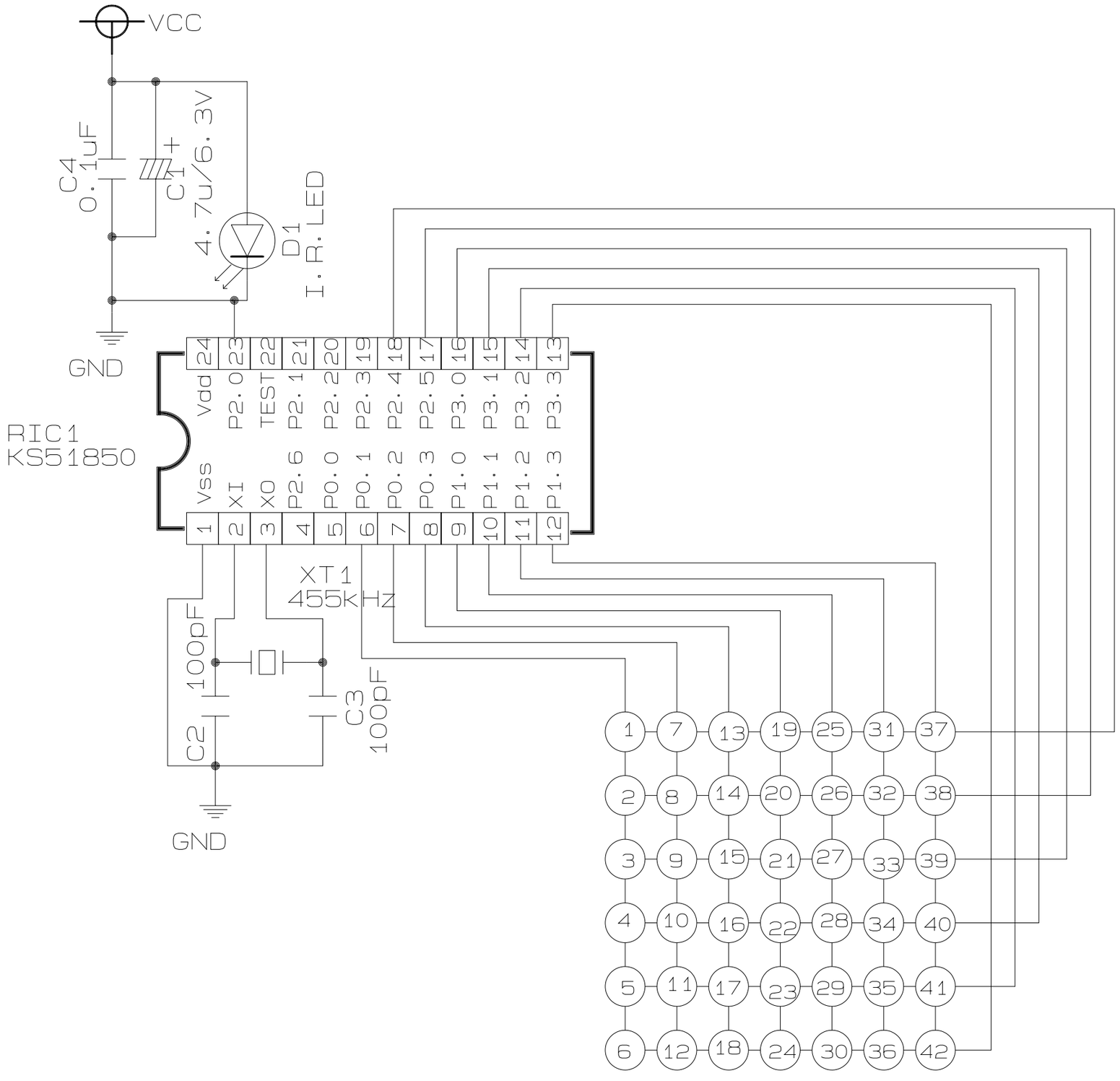
13-10 Key


CON21
S7
6
S8
5
KEY0
4
KEY1
3
KEY2
2
DGND
1
TO/FROM
FRONT
CN3
FSW6
SKIP/SEARCH
FSW1
SKIP/SEARCH
FSW2
OPEN/CLOSE
FSW4
PLAY
FSW5
STOP
DGND

13-11 Deck


CN2
E 1
A 2
D 3
RF 4
C 5
B 6
F 7
VCC 8
VREF 9
GND_PD 10
T− 11
T+ 12
F+ 13
F− 14
GND_BODY 15
GND−DLD 16
DVDLD 17
VOL_DVD 18
DVDPD 19
VCC 20
TO/FROM PICK-UP
DD2 1N4148
DC4 103
DC1 103
DC2 103
SW3 LDON/OFF
DR7 220
VCC
DR5 180
CN3
H+ 1
HW− 2
HW+ 3
HV− 4
HV+ 5
HU− 6
HU+ 7
H− 8
U 9
V 10
W 11
TO/FROM SINDLE MOTOR
DR4 180
GND
DJP5 JUMPER
2LD/1LD
GND
TO TRAY MOTOR
TM+
TM−
TO SLED MOTOR
SLED+
SLED−
VCC
DR1 10K
DR6 10K
SW1 OPEN
OPSW
SW2 CLOSE
CLSW
GND
DC5 103
CN1
1 E
2 F
3 D
4 C
5 RF
6 B
7 A
8 GND
9 GND
10 T−
11 F+
12 T+
13 F−
14 GND
15 CDLD
16 CDPD
17 GND
18 VREF
19 VCC
20 VCC
21 DVDLD
22 DVDPD
23 GND
24 HW+
25 HW−
26 HV−
27 HU−
28 V
29 W
30 U
31 HU+
32 HV+
33 GND
34 TM+
35 TM−
36 CLSW
37 OPSW
38 1/2LD
39 SLED+
40 SLED−
TO/FROM RF DCN1

13-12 Remote Control



MEMO

HITACHI

DV-P305U/P303U

DV-P305U
DV-P303U

TK No.9003E Digital Media Products Division, Tokai

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Printed in Japan (II)